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UNITED STATES DEPARTMENT OF COMMERCE
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July 07, 2003

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APPLICATION NUMBER: ***60/398,860***
FILING DATE: ***July 25, 2002***
RELATED PCT APPLICATION NUMBER: *PCT/US03/18129*

By Authority of the
COMMISSIONER OF PATENTS AND TRADEMARKS

E. Bornett

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Certifying Officer

7-25-02

PTO/SB/16 (8/96)
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Attorney Docket No. 001340.P086Z2

Type a plus sign (+) inside this box [+]

PROVISIONAL APPLICATION FOR PATENT COVER SHEET

This is a request for filing a PROVISIONAL APPLICATION FOR PATENT under 37 CFR 1.53 (c).

INVENTOR(s)/APPLICANT(s)

LAST NAME	FIRST NAME	MIDDLE NAME/ INITIAL	RESIDENCE (CITY AND EITHER STATE OR FOREIGN COUNTRY)
Tsatsanis	Michail		
Erickson	Mark		
Kanellakopoulos	Ioannis		

TITLE OF THE INVENTION (280 characters max)

A METHOD AND SYSTEM FOR MULTI-LINE TRANSMISSION IN A COMMUNICATIONS SYSTEM

CORRESPONDENCE ADDRESS (including country if not United States)

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ENCLOSED APPLICATION PARTS (check all that apply)

X	Specification	Number of Pages 114		Small Entity Statement
	Drawing(s)	Number of Sheets	X	Other (specify) Express Mail Certification

METHOD OF PAYMENT OF FILING FEES FOR THIS PROVISIONAL APPLICATION FOR PATENT (check one)

X A check or money order is enclosed to cover the filing fees

The Commissioner is hereby authorized to charge filing fees and credit Deposit Account No. 02-2666

Filing Fee Amount ($) 160.00

This invention was made by an agency of the United States Government or under contract with an agency of the United States Government..

X No

Yes, the name of the U.S. Government Agency and the Government Contract Number are:

Respectfully submitted,

SIGNATURE Glenn E. Von Tersch DATE July 25, 2002

TYPED or PRINTED NAME: Glenn E. Von Tersch REGISTRATION NO. 41,364 (If appropriate)

X Additional inventors are being named on separately numbered sheets attached hereto

USE ONLY FOR FILING A PROVISIONAL APPLICATION FOR PATENT

Address to: Box Provisional Application, Assistant Commissioner for Patents, Washington, D. C. 20231

PROVISIONAL APPLICATION COVER SHEET
Additional Page

Attorney Docket No. 001340.P086Z2

Type a plus sign (+) inside this box [+]

INVENTOR(s)/APPLICANT(s)

LAST NAME	FIRST NAME	MIDDLE NAME/ INITIAL	RESIDENCE (CITY AND EITHER STATE OR FOREIGN COUNTRY)
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Mukherjee	Aditya		
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Cardanha	Brian		

PTO/SB/17(09/00)
Approved for use through 10/31/2002. OMB 0651-0032
Patent and Trademark Office: U.S. DEPARTMENT OF COMMERCE

FEE TRANSMITTAL FOR FY 2002

TOTAL AMOUNT OF PAYMENT ($) $160.00

Complete If Known:

Application No.	New Provisional Patent Application
Filing Date	Herewith
First Named Inventor	Michail Tsatsanis
Group Art Unit	Not Yet Assigned
Examiner Name	Not Yet Assigned
Attorney Docket No.	001340.P086Z2

METHOD OF PAYMENT (check one)

1. [X] **The Commissioner is hereby authorized to charge indicated fees and credit any over payments to:**

   Deposit Account Number 02-2666
   Deposit Account Name Blakely, Sokoloff, Taylor & Zafman

   [X] **Charge Any Additional Fee Required Under 37 CFR 1.16 and 1.17**

   [ ] **Applicant claims small entity status. See 37 CFR 1.27**

2. X **Payment Enclosed:** X **Check**
   ____ **Money Order**
   ____ **Other**

FEE CALCULATION

1. **BASIC FILING FEE**

Large Entity Fee Code	Large Entity Fee ($)	Small Entity Fee Code	Small Entity Fee ($)	Fee Description	Fee Paid
101	740	201	370	Utility application filing fee	
106	330	206	165	Design application filing fee	
107	510	207	255	Plant filing fee	
108	740	208	370	Reissue filing fee	
114	160	214	80	Provisional application filing fee	160.00

SUBTOTAL (1) $160.00

2. **EXTRA CLAIM FEES**

		Extra Claims		Fee from below		Fee Paid
Total Claims	____	– 20** =	____	X ____	=	____
Independent Claims	____	– 3** =	____	X ____	=	____
Multiple Dependent				____	=	____

**Or number previously paid, if greater; For Reissues, see below.

Large Entity Fee Code	Large Entity Fee ($)	Small Entity Fee Code	Small Entity Fee ($)	Fee Description
103	18	203	9	Claims in excess of 20
102	84	202	42	Independent claims in excess of 3
104	280	204	140	Multiple dependent claim, if not paid
109	84	209	42	**Reissue independent claims over original patent
110	18	210	9	**Reissue claims in excess of 20 and over original patent

SUBTOTAL (2) $0

FEE CALCULATION (continued)

3. ADDITIONAL FEES

Large Entity Fee Code	Large Entity Fee ($)	Small Entity Fee Code	Small Entity Fee ($)	Fee Description	Fee Paid
105	130	205	65	Surcharge - late filing fee or oath	
127	50	227	25	Surcharge - late provisional filing fee or cover sheet	
139	130	139	130	Non-English specification	
147	2,520	147	2,520	For filing a request for ex parte reexamination	
099	8,800	099	8,800	Request for inter parties reexamination	
112	920*	112	920*	Requesting publication of SIR prior to Examiner action	
113	1,840*	113	1,840*	Requesting publication of SIR after Examiner action	
115	110	215	55	Extension for reply within first month	
116	400	216	200	Extension for reply within second month	
117	920	217	460	Extension for reply within third month	
118	1,440	218	720	Extension for reply within fourth month	
128	1,960	228	980	Extension for reply within fifth month	
119	320	219	160	Notice of Appeal	
120	320	220	160	Filing a brief in support of an appeal	
121	280	221	140	Request for oral hearing	
138	1,510	138	1,510	Petition to institute a public use proceeding	
140	110	240	55	Petition to revive – unavoidable	
141	1,280	241	640	Petition to revive - unintentional	
142	1,280	242	640	Utility issue fee (or reissue)	
143	460	243	230	Design issue fee	
144	620	244	310	Plant issue fee	
122	130	122	130	Petitions to the Commissioner	
123	50	123	50	Processing fee under 37 CFR 1.17(q)	
126	180	126	180	Submission of Information Disclosure Stmt	
581	40	581	40	Recording each patent assignment per property (times number of properties)	
146	740	246	370	For filing a submission after final rejection (see 37 CFR 1.129(a))	
148	110	248	55	Statutory Disclaimer	
149	740	249	370	For each additional invention to be examined (see 37 CFR 1.129(b))	
179	740	279	370	Request for Continued Examination (RCE)	
169	900	169	900	Request for expedited examination of a design application	
195	300	195	300	Publication fee for early, voluntary, or normal pub.	
196	300	196	300	Publication fee for republication	
194	130	194	130	Request for voluntary publication or republication	
098	130	098	130	Processing fee under 37 CFR 1.17(i) (except provisionals)	
091	1,280	091	1,280	Acceptance of unintentionally delayed claim for priority	

Other fee (specify) _____

Other fee (specify) _____

SUBTOTAL (3) $ 0

*Reduced by Basic Filing Fee Paid

SUBMITTED BY:

Typed or Printed Name: Glenn E. Von Tersch

Signature: _____ Date: July 25, 2002

Reg. Number: 41,364 Telephone Number: (408) 720-8300

PROVISIONAL PATENT

UNITED STATES PROVISIONAL PATENT APPLICATION

FOR

A METHOD AND SYSTEM FOR MULTI-LINE TRANSMISSION IN A COMMUNICATIONS SYSTEM

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Date of Deposit July 25, 2002

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Carrie Boccaccini
(Typed or printed name of person mailing paper or fee)

Carrie Boccaccini 7-25-2002
(Signature of person mailing paper or fee) Date

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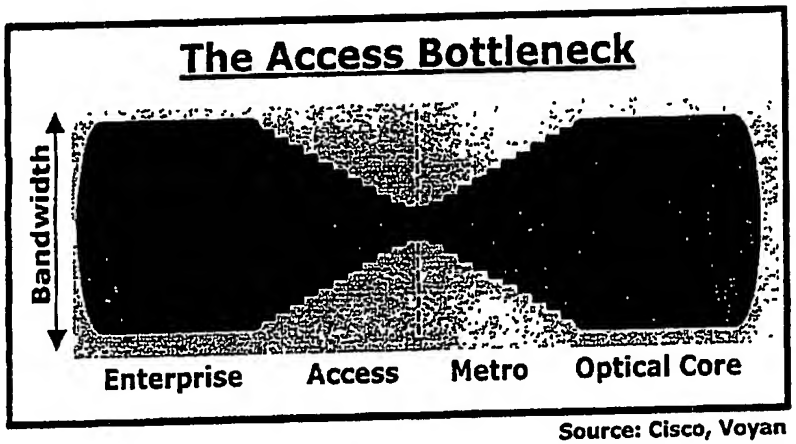
Broadband in the Last Mile
Increasing Customer Demand

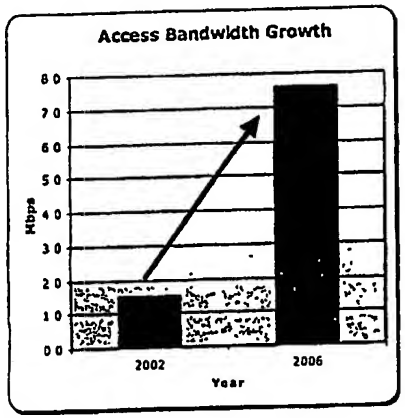


Source: Cisco, Voyan

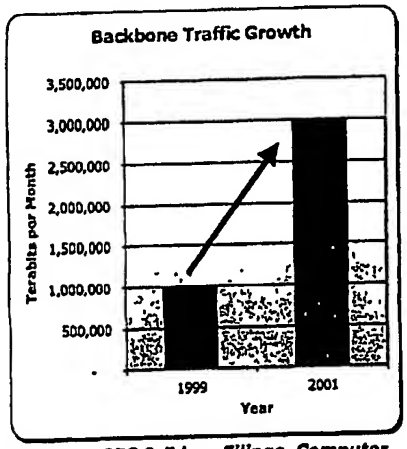
- **Bandwidth expansion has been bipolar**
  - **Enterprise Networks**
    - 10 Mbps -> 100 Mbps -> Gigabits
  - **Optical Core Network**
    - -> 40 Gbps
    - immense available capacity
  - **Access & Metro Networks have NOT kept pace**
    - 1.5Mbps is the fastest available service offered to most businesses today

Market Drivers

Growing Demand for Bandwidth



Source: Gartner Group



Source: SEC & Edgar Filings, Computer Industry Almanac, Intel

Access bandwidth demand is growing

- **25% - 50% CAGR for the average enterprise[1]**
- **Much higher for some applications[2]**

Demand for broadband access is widespread geographically

Backbone traffic has grown at > 70% CAGR

- **1999: 1,000,000 terabits / month[3]**
- **2001: 3,000,000 terabits / month[3]**

Notes

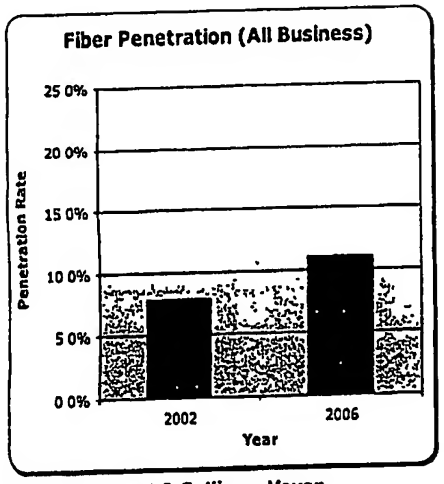
1 Gartner Group; Look Out WAN – The Ethernet Roadkill Machine is Coming; Research note COM-12-9201; Jay Pultz and Mark Fabb; February 6, 2001

2 Lehman Brothers; Enterprise Storage Takes Center Stage; February 12, 2001

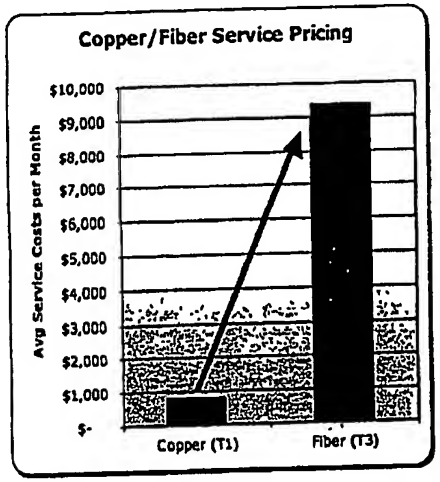
3 Sources: SEC & Edgar Filings, Computer Industry Almanac, Intel

Market Inhibitors

Copper Performance/Fiber Availability and Cost



Source: Frost & Sullivan, Voyan



Source: Frost & Sullivan

Copper infrastructure is ubiquitous but current technology delivers only limited performance

Fiber penetration is low relative to all businesses and is limited to certain geographic areas

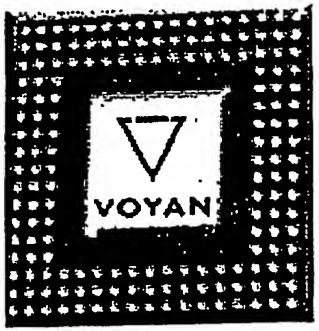
Capital budgets are tight and fiber is costly to deploy in many situations

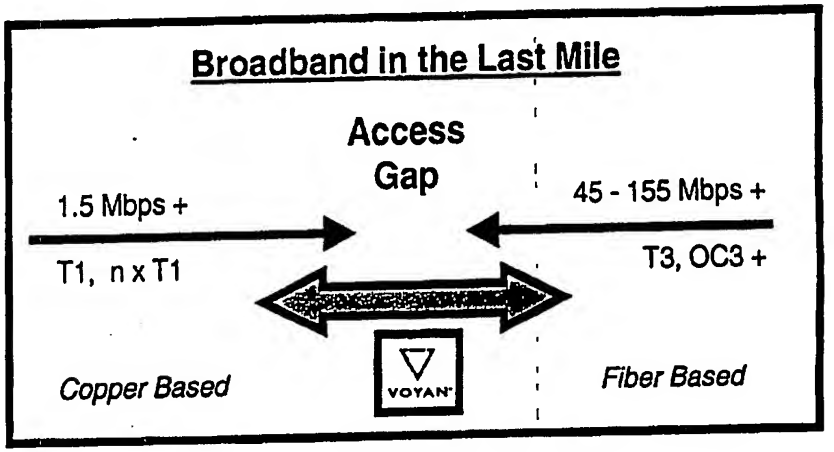
Based on high costs for deployment, fiber based services are ~ 12x the cost of copper based services

Together, these conditions have created an "Access Gap"

Introducing *OptiFusion*

Solving the "Access Gap" Problem



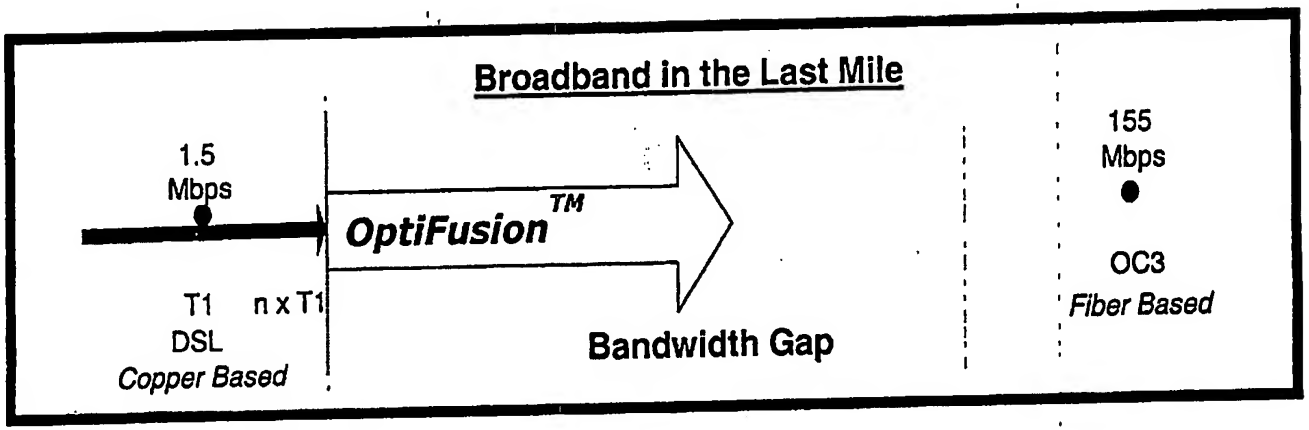


A chipset solution offering fiber-like performance levels to be achieved using the existing copper infrastructure

Bridges the gap between copper-based and fiber-based services in a cost effective way

Delivers T1, FT3, T3 and multi-megabit packet services for a wide variety of carrier applications

Broadband in the Last Mile
OptiFusion™ enables Broadband



- ***OptiFusion™* fills the Bandwidth Gap**
  - **Maximizes potential of existing copper access network**
    - Increases the average throughput per pair
    - Operates over the full CSA range
      - 9000ft - 26AWG
      - 12000ft - 24AWG
    - Enables service offerings previously only available over costly fiber
      - 10Mbps over 4 copper pairs (Ethernet service)
      - 45Mbps over 10 copper pairs (T3 service)
    - Requires no access line grooming
      - Robust performance in the presence of other co-located services (even same binder)
      - Spectrally friendly to other co-located services (even same binder)

OptiFusion Value Proposition

Maximize carrier revenue and penetration by enabling high speed, high tariff services to be delivered cost effectively and ubiquitously with the existing copper infrastructure.

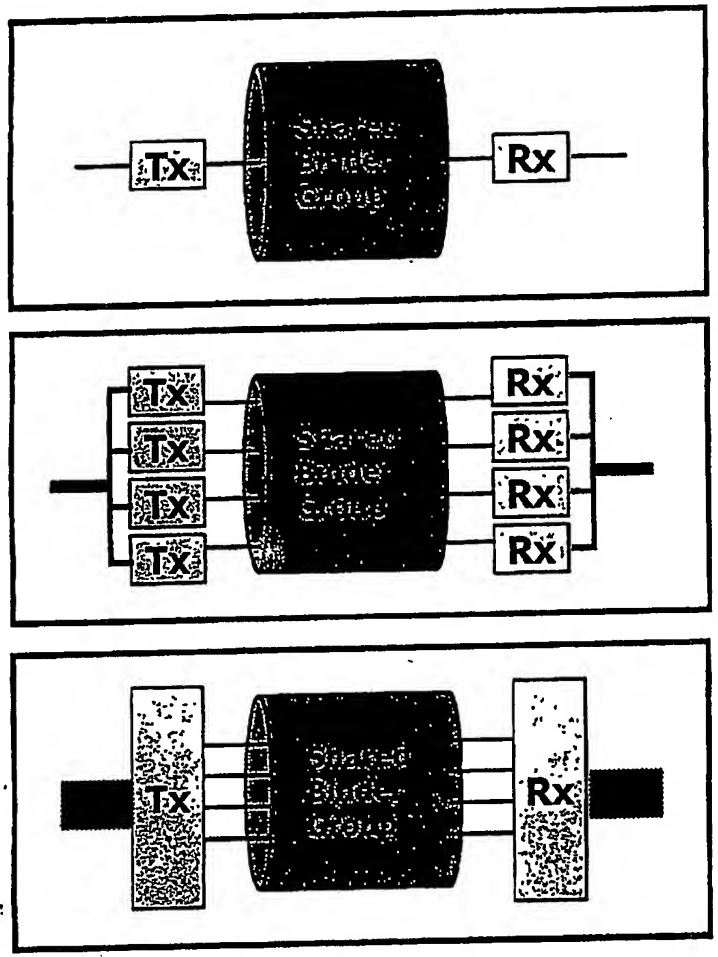
Operates on existing copper infrastructure	Minimizes capital investment Widespread deployment potential
Delivers high symmetrical speeds to full CSA	Greater customer penetration Significant revenue growth
Scalability	Flexible service definitions and provisioning
Quick service activation	Fast revenue recognition Satisfied customers
Spectrally friendly	Operates w/ other services in binder Will not impact other services in binder

OptiFusion Technology
Components

Symmetric	Enables business service delivery
DMT Line Code	Proven Widely deployed Cost effective
G.SHDSL Spectral Mask	Industry standard Deployable today Symmetric
Vectored multi-line transmission using MIMO signal processing techniques	Proven in wireless applications Characterizes and mitigates crosstalk Bonding at the physical layer ▪ No overhead ▪ Reduced latency

DMT – Discrete Multitone Transmission
MIMO – Multiple Input Multiple Output

Copper Transmission Systems



Single Line

- Single Input Single Output system (SISO)
- Examples: ADSL, VDSL, G.SHDSL

Traditional Multi-line

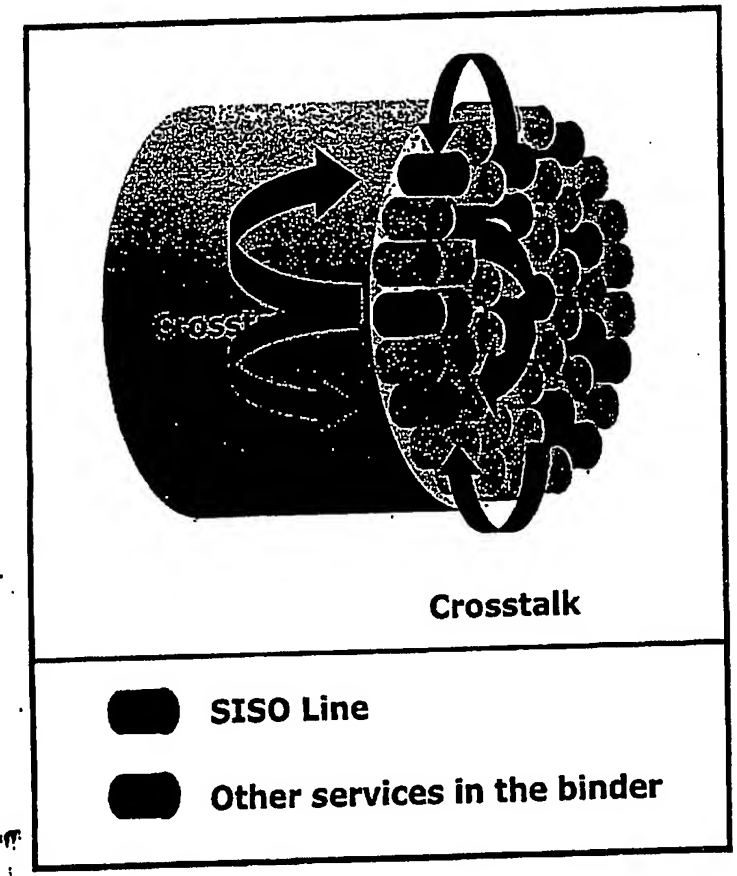
- Collection of individual SISO's
- Each SISO acts independently
- Essentially a multiple SISO system

Vectored Multi-line

- Multiple Input Multiple Output system (MIMO)
- Transmission across individual lines is coordinated

Crosstalk in Single Line Systems

Basics



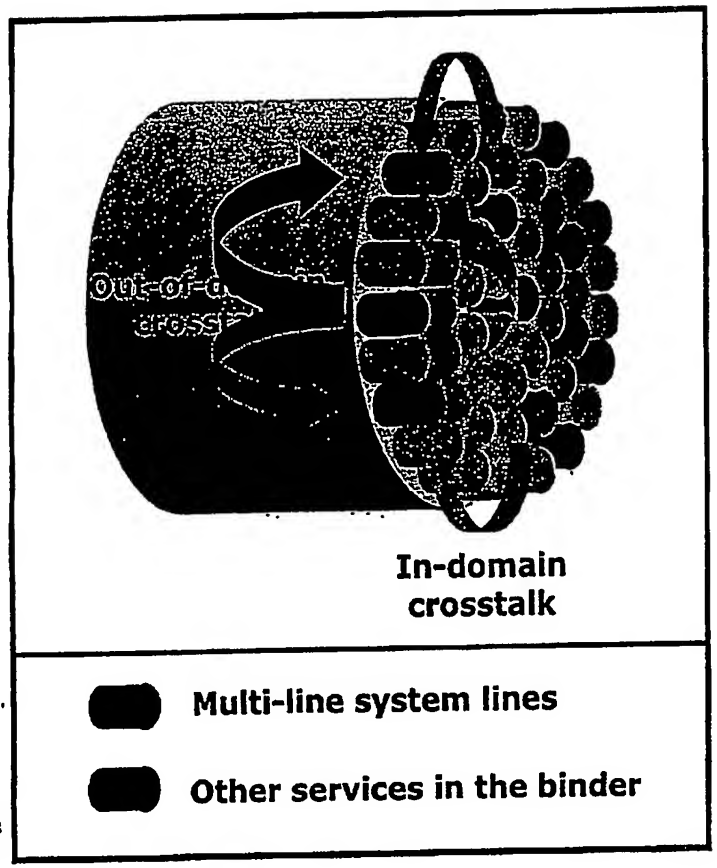
Crosstalk is the major cause of performance impairment in copper transmission systems

In copper binders all lines interfere with one another

SISO transmission throughput is restricted to compensate for unknown crosstalk

Crosstalk in Multi-line Systems

Traditional Technologies



Traditional multi-line transmission aggregates multiple SISO systems together

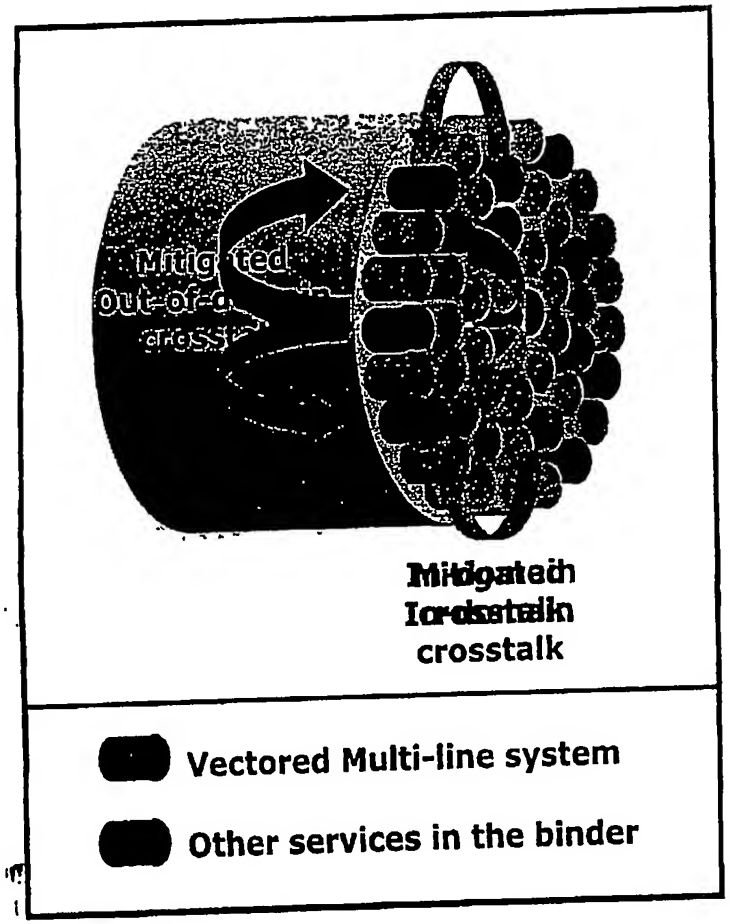
Crosstalk remains unchecked

- **In-domain crosstalk**
  Between the individual SISO lines themselves
- **Out-of-domain crosstalk**
  From other services in the binder

Throughput still restricted to compensate for unknown impairments

Crosstalk in Multi-line Systems

The *OptiFusion* Approach



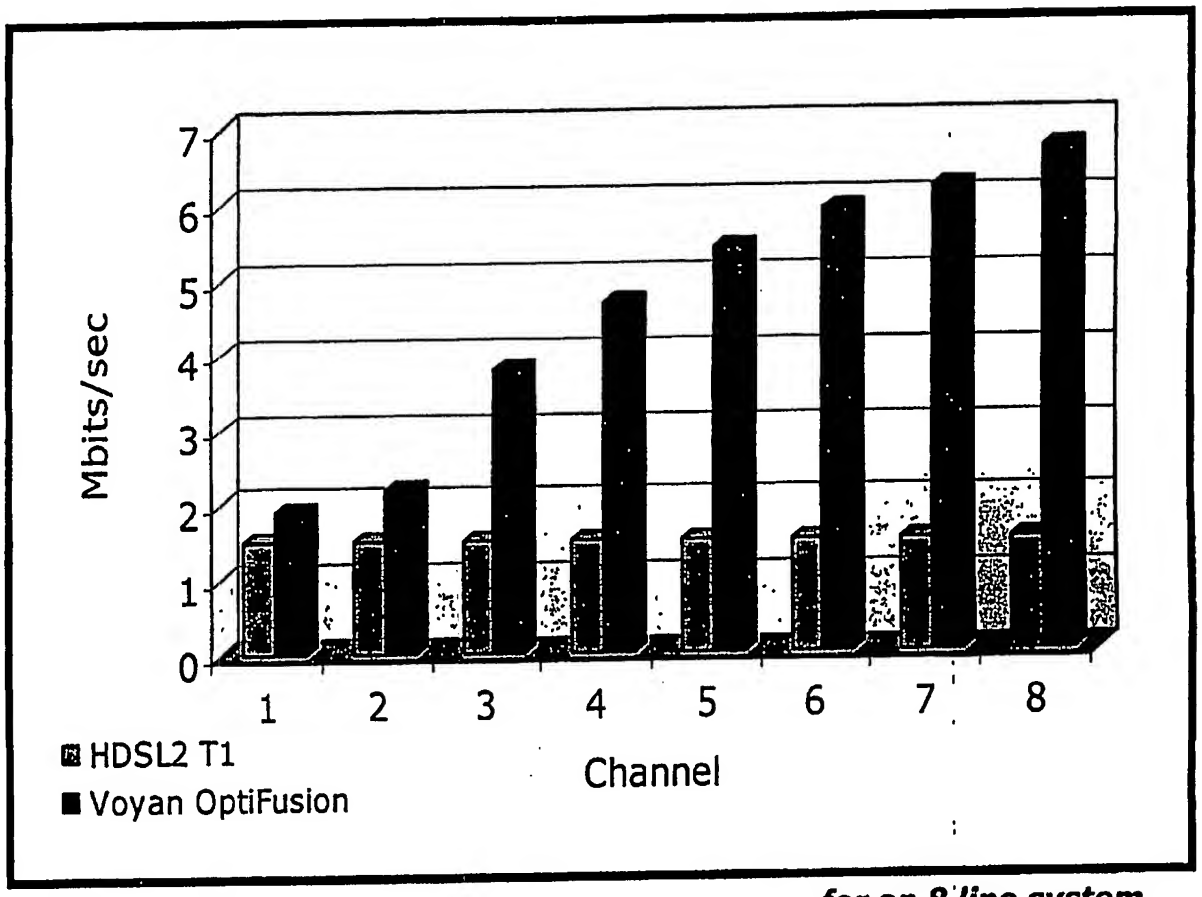
Vectored multi-line transmission

- **Characterize and mitigate for in-domain crosstalk**
- **Characterize and mitigate for out-of-domain crosstalk**

Enables dramatic improvement in performance

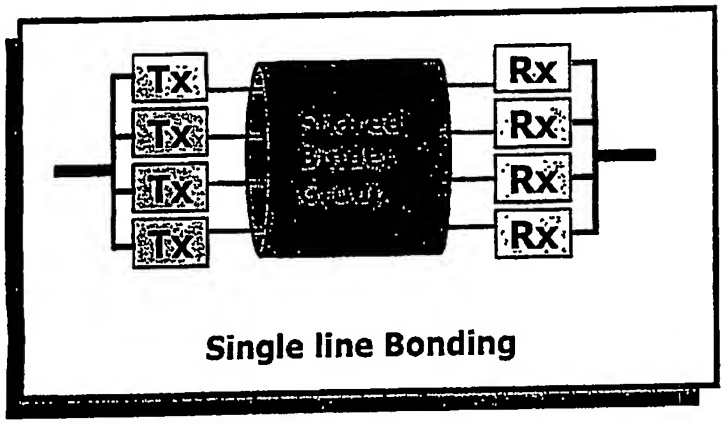
OptiFusion Technology

Removing the Constraints of Crosstalk



for an 8 line system

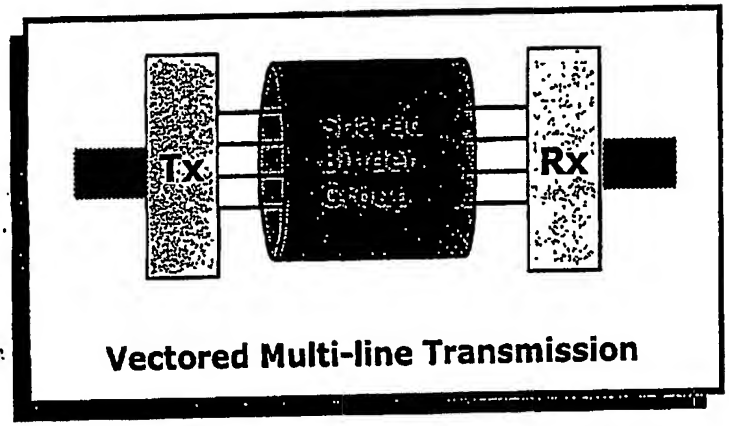
OptiFusion
Bonding at the Physical Layer



Single line Bonding

Single line bonding

- Unpacking & repacking data at either end of each single transmission line incurs
  - Overhead
  - Latency
- The aggregate throughput is less than the sum of the parts



Vectored Multi-line Transmission

Vectored Multi-line transmission

- Bonding at the physical layer
  - without frames/cells
  - with minimal delay
- Maximum use of the available bandwidth

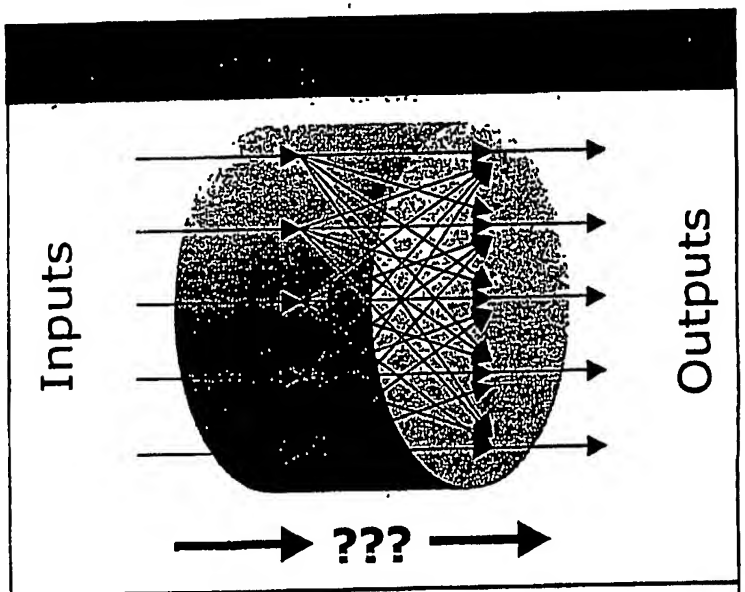
The *OptiFusion* Difference

Vectored multi-line transmission ...

- Treating multiple lines together as one system rather than treating the lines individually
- Vectored – the mathematical concept introduced by processing signals across multiple lines

... using MIMO signal processing techniques

- Signaling techniques for obtaining an understanding of what is occurring within a complex system involving many inputs and outputs

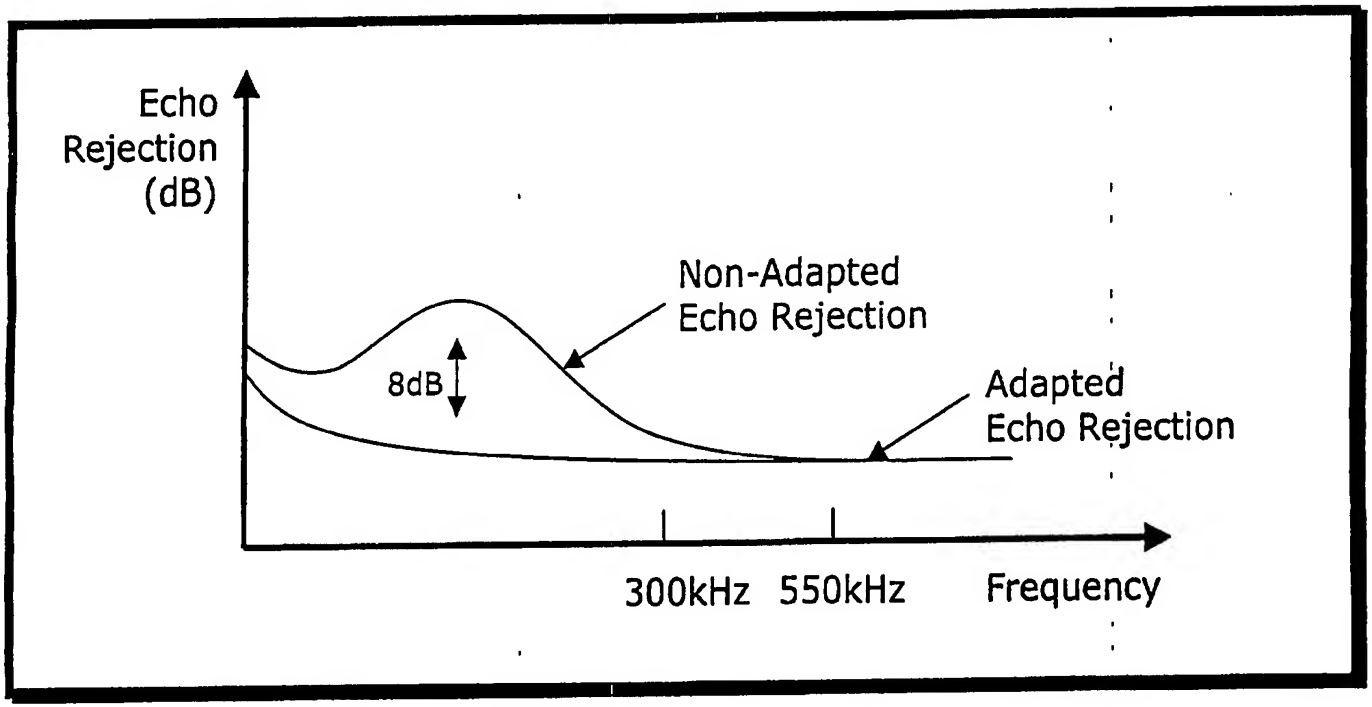


Real-life binder systems are dynamically complex and non-linear

Outputs affected by unknown and variable disturbances

Every input affects every output

OptiFusion™ Adaptation Gains

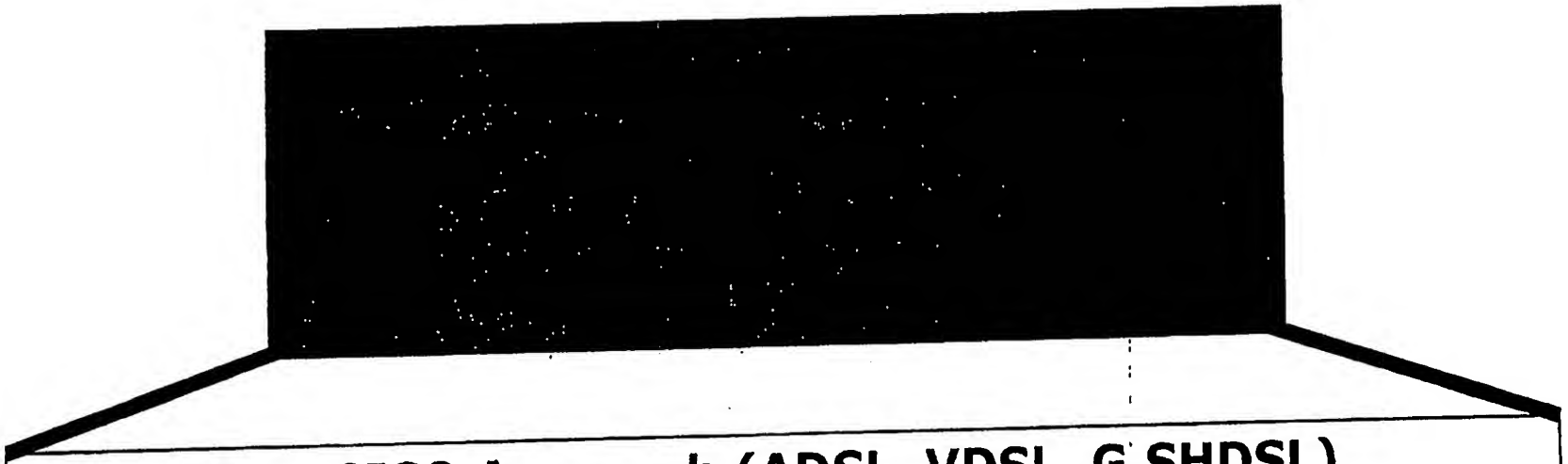


avg. 8dB over 300kHz bandwidth / 3dB per bps per Hz

8/3 x 300k x 8 Channels = 6.4Mbps

OptiFusion

The Next Level in Performance



The SISO Approach (ADSL, VDSL, G.SHDSL)

SISO techniques have essentially reached their practical performance limits

Proposed improvements are for short loops and offer only incremental gains

Multi-line SISO implementations do not offer performance gains

Technology Demonstration

What Will Be Demonstrated?

Voyan's *OptiFusion* Technology

- A novel vectored multi-line transmission method leveraging MIMO signal processing techniques
- Dramatically increases achievable rate and reach performance of the existing copper infrastructure

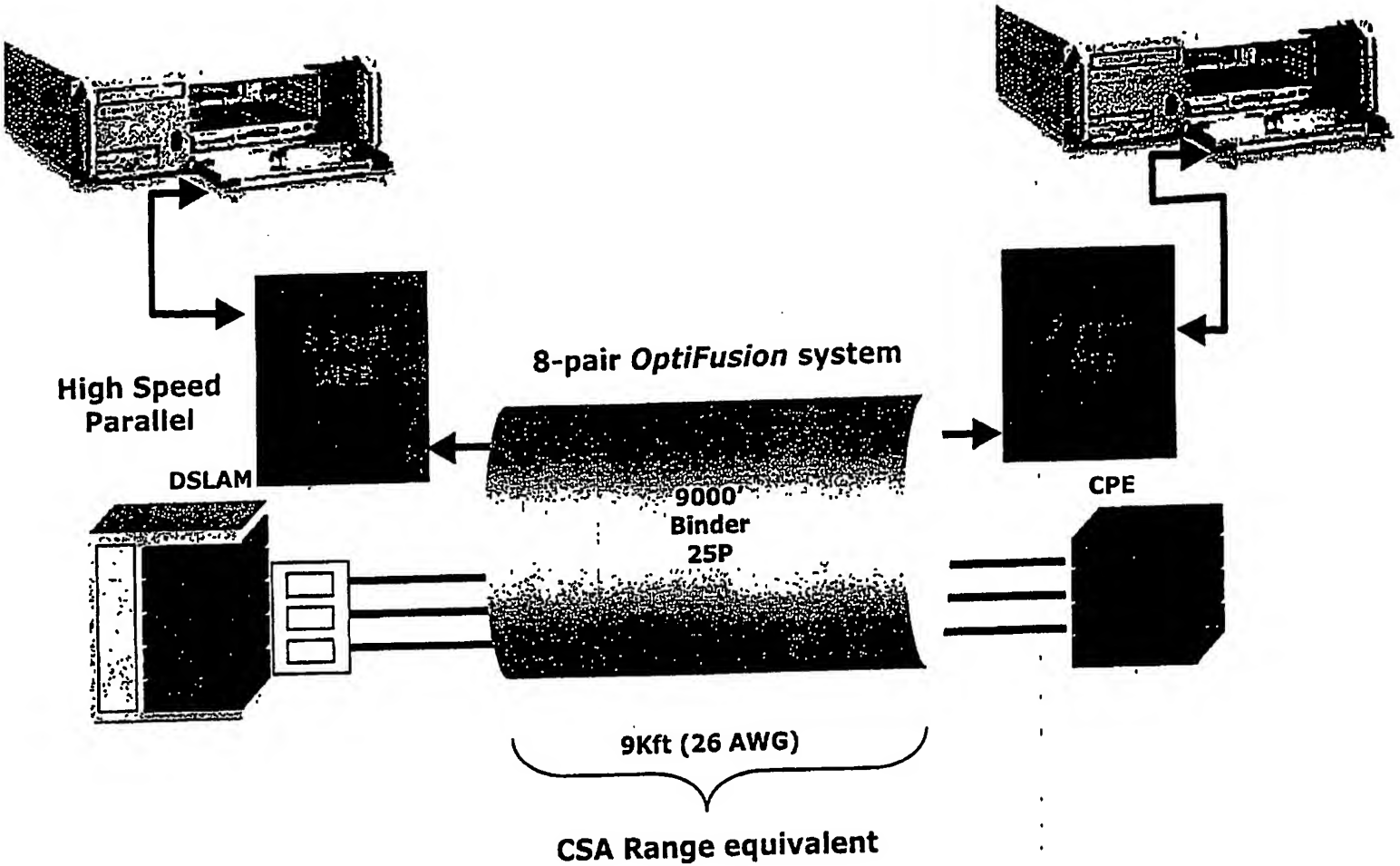
Today

- The first hardware demonstration ever of vectored MIMO technology in a wireline application

MIMO = Multi Input Multi Output

Technology Demonstration

Lab Setup



OptiFusion™ Demonstration Performance Targets

	Disturber Set	
	Scenario A	Scenario B
9kft 26AWG 8 pairs	[redacted]	

Disturber Services	Disturber Set	
	Scenario A	Scenario B
ADSL	3	1
SDSL (HDSL)	4	2
HDSL2	2	1
VDSL	1	1
DDS	1	0
IDSL	1	0
# ext. disturber pairs	13	5
# SELF disturber pairs	7	7
Total disturbers	20	12

Technology Demonstration

Timeline

Training Stages

Echo Cancellation

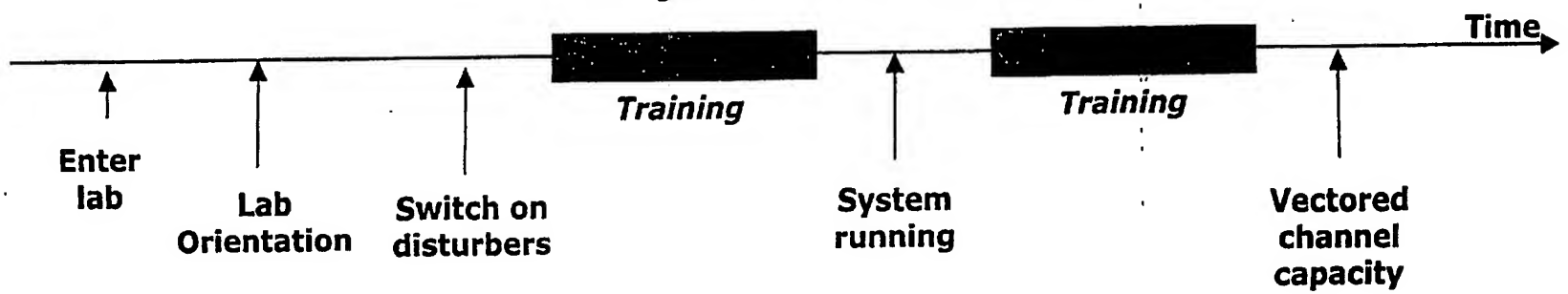
Clock Acquisition
(Downstream side only)

Time Equalizers

Frequency Equalizers

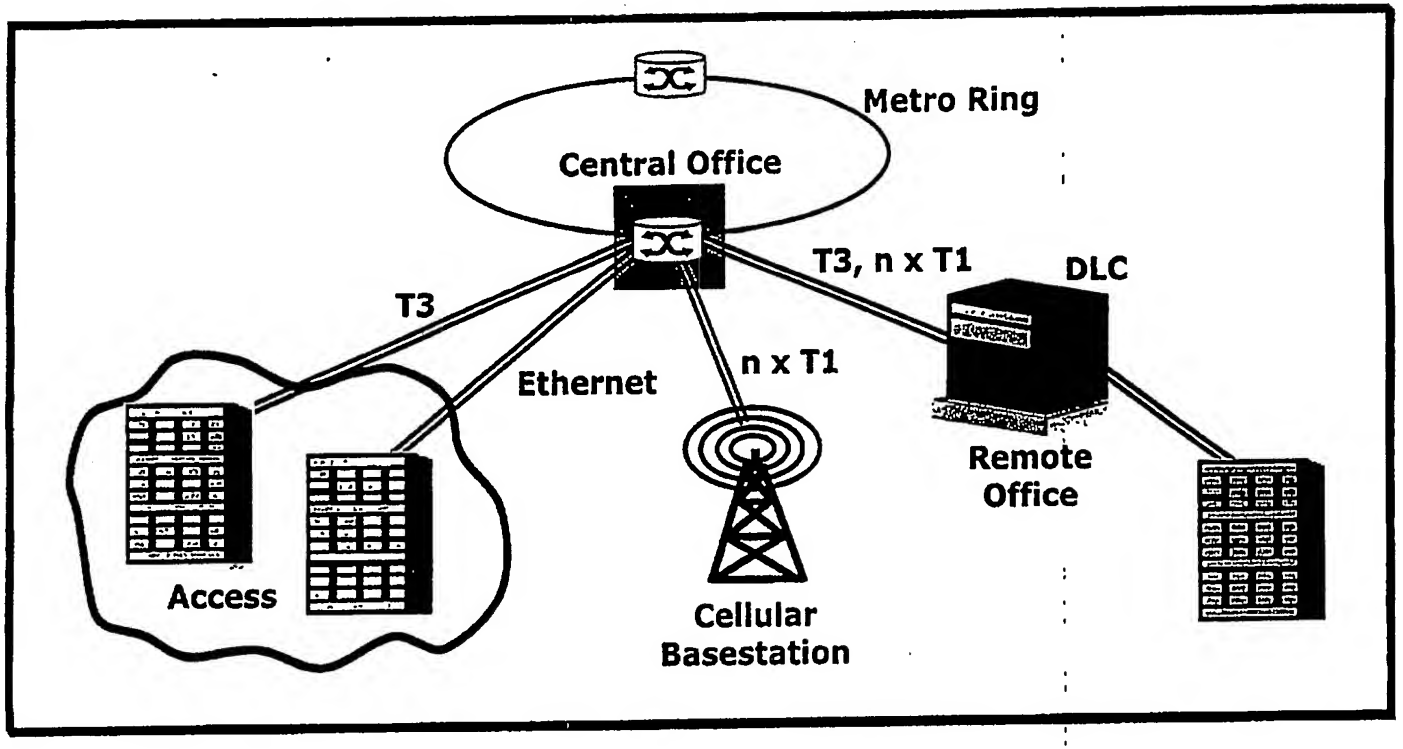
MIMO Processing Parameters

Bit-loading Calculation



OptiFusion Product Plans

Three Speed/Service Classes



T3 solution

- Delivers T3 and fractional service over 10 pairs (at TDM performance levels)

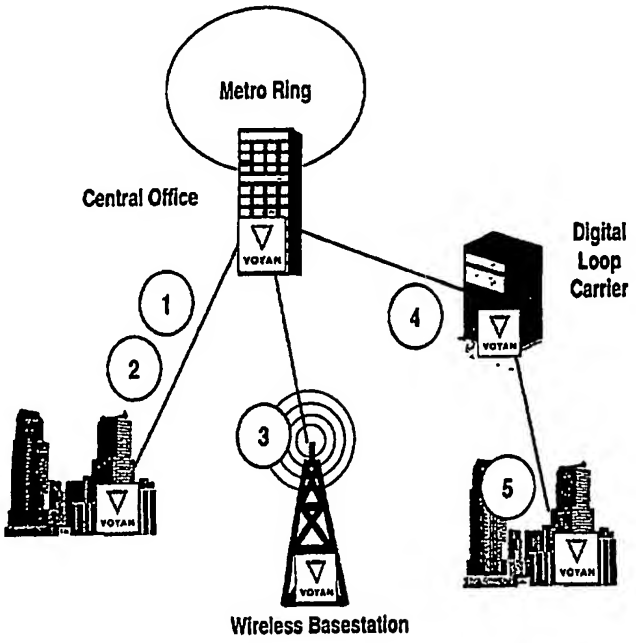
Ethernet solution

- Delivers 10 Mbps packet service over 3-4 pairs

n x T1/E1 solution

- Deliver up to 7 x T1 over 4 pairs (at TDM performance levels)

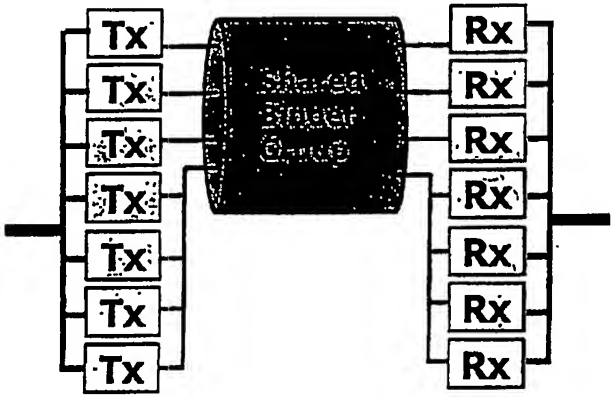
OptiFusion Applications



OptiFusion Network Applications	
1	***Access*** **Affordable T3, FT3, n x T1, Ethernet private line and packet services**
2	***Pair Gain*** **n x T1 for copper constrained routes and next generation packet services such as IMA and multilink Frame Relay**
3	***Wireless*** **Base station backhaul for supporting 2.5G and 3G wireless data services**
4	***DLC*** **Digital Loop Carrier (DLC) backhaul for enabling broadband services on the customer side**
5	***Campus/Enterprise*** **Lengthy copper runs which cannot be handled by traditional methods**

10 Mbps Ethernet

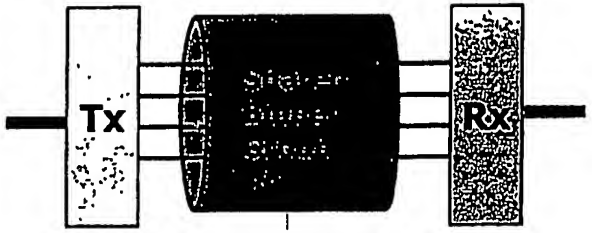
OptiFusion vs. G.SHDSL



G.SHDSL System

7 x T1 Bonded System

- Multiple SISO systems offer no synergistic performance gains
- Higher overhead and latency
- 7 copper pairs required for 10 Mbps service



***OptiFusion* System**

OptiFusion System

- Vectored MIMO system offers substantial performance gains
- Minimal overhead and latency
- 4 copper pairs required for 10 Mbps service

Better Performance & Fewer Pairs

10 Mbps Ethernet

OptiFusion vs. VDSL

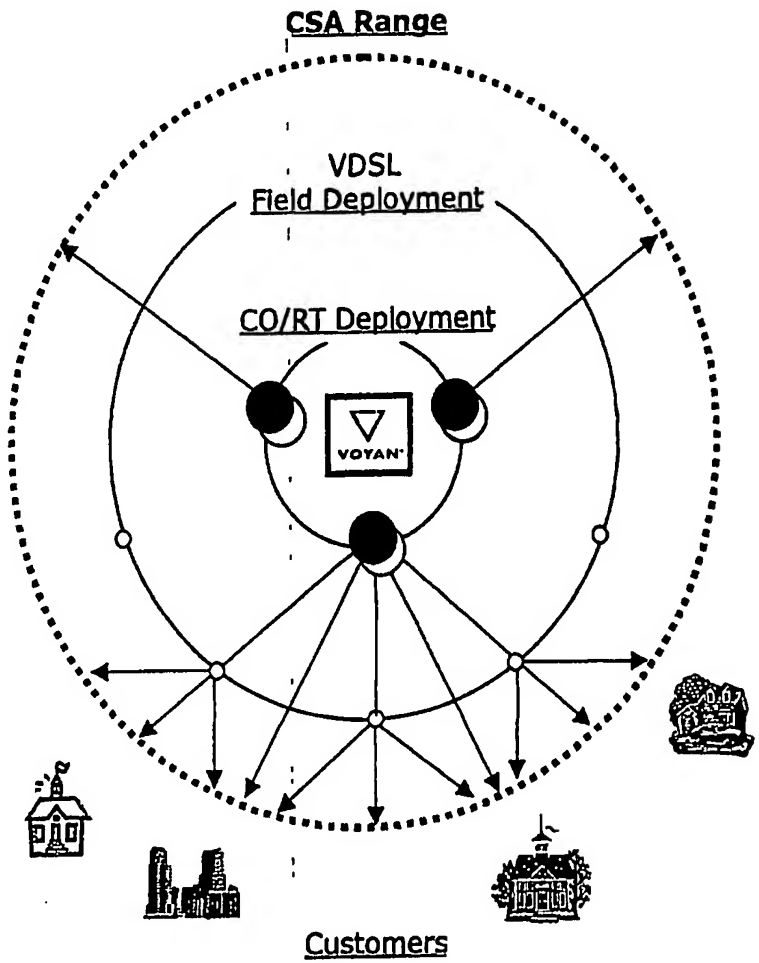
○ VDSL Solution

- Limited reach – too many systems
- Higher capital and operating costs for systems, infrastructure, support and logistics

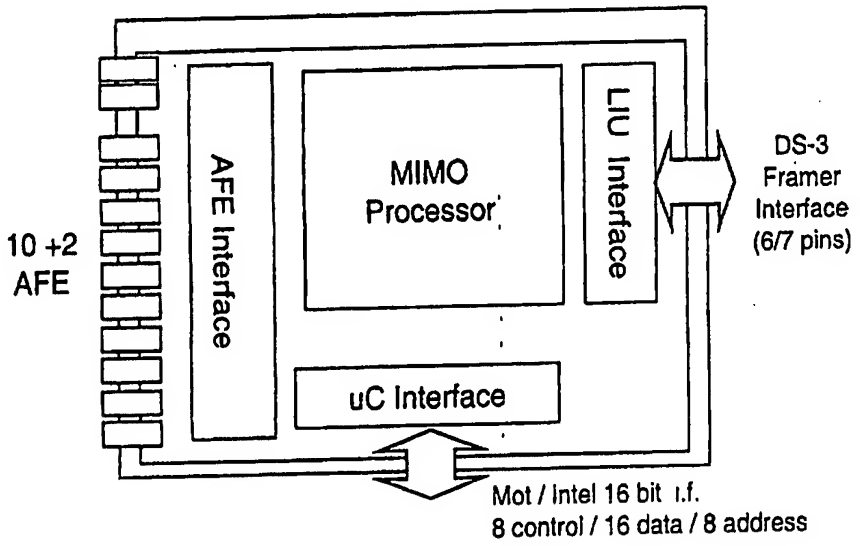
● OptiFusion Solution

- Great reach – fewer systems
- Minimal capital and operating cost impact

Broad Coverage & Lower Cost



T3 over Copper Product Features



Applications

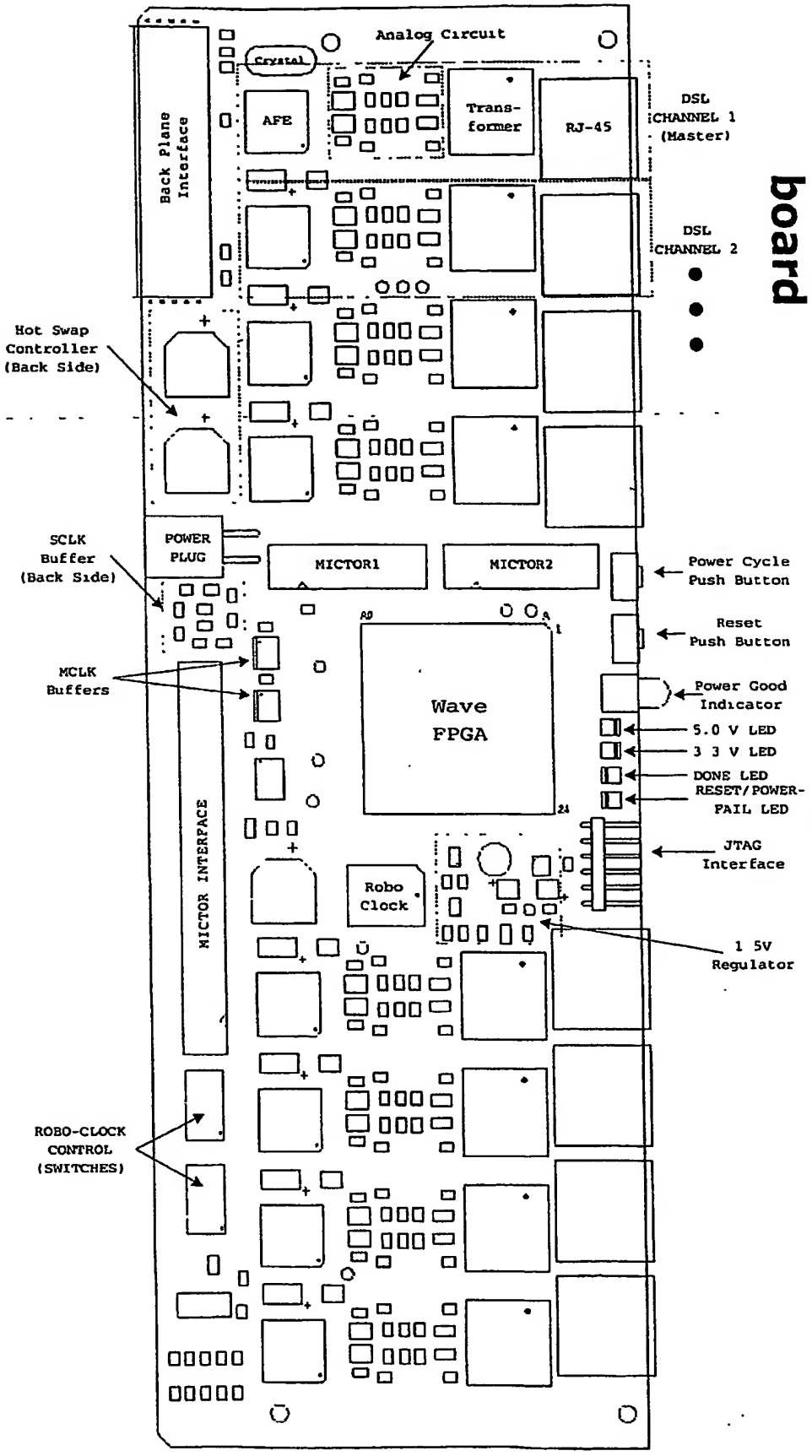
- T3 Access Equipment
- DLC Backhaul
- Next Generation (3G) Base Stations

Features

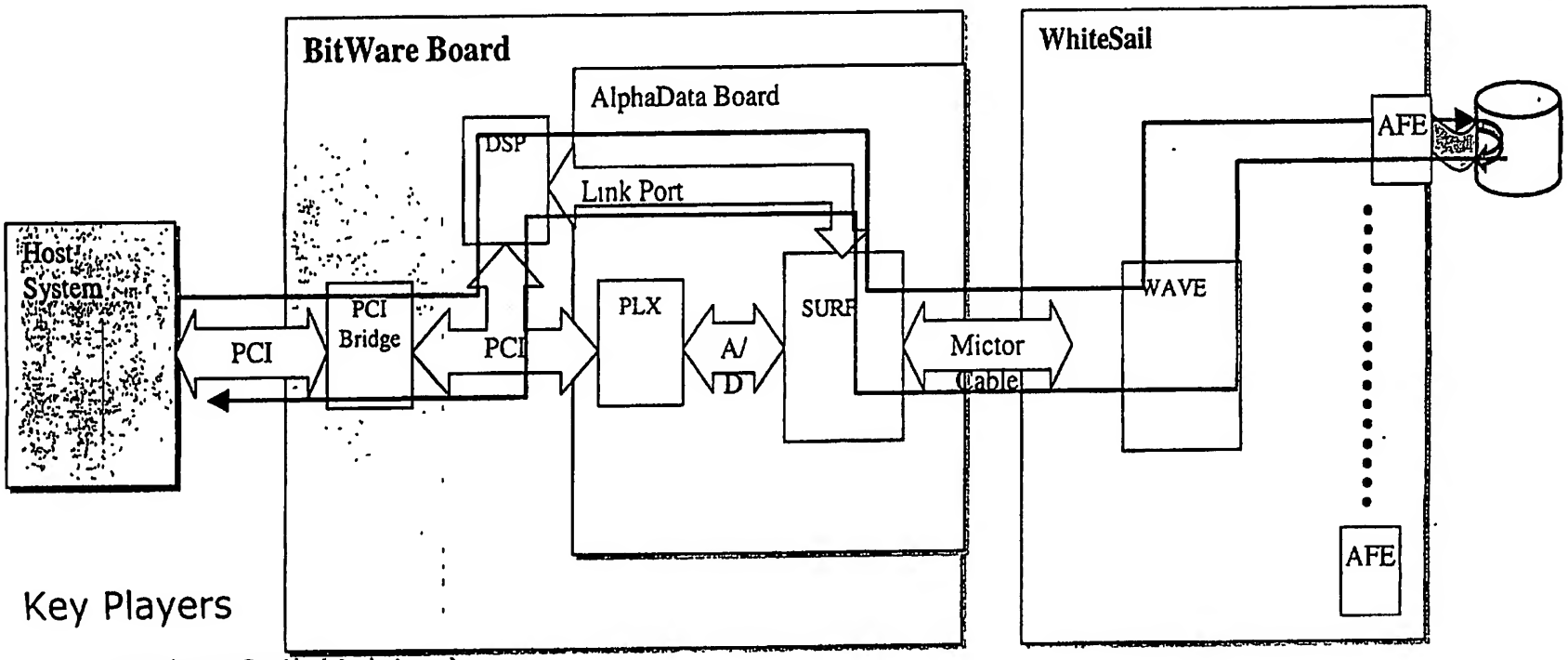
- **Line Interface Unit (LIU) chipset**
  - T3 (44.7Mbps) / E3 (34.368 Mbps)
  - over 10 twisted copper pair
  - at CSA range
- **Fractional T3 services supported**
- **Scalable provisioning –**
  - service can be provisioned over fewer pairs at shorter range
- **Spectral compatibility according to T1.417**
- **Full toll voice service**
- **End to end latency: 1ms**
- **On-chip training and adaptation**

What's WhiteSail?

- CompactPCI 6U rear form factor 8 channel AFE board



WhiteSail in POC System



Key Players

- WhiteSail (Adrian)
- WAVE (Satish)
- SURF (Norm)
- Test Plans & Bring-up Collateral (Brian)
- Timing, P&R (Johan)
- Fast Track Purchase Orders !! (Cristine)

WAVE ARCHITECTURE DOCUMENT

TABLE OF CONTENTS

1 IS /-IS NOT List

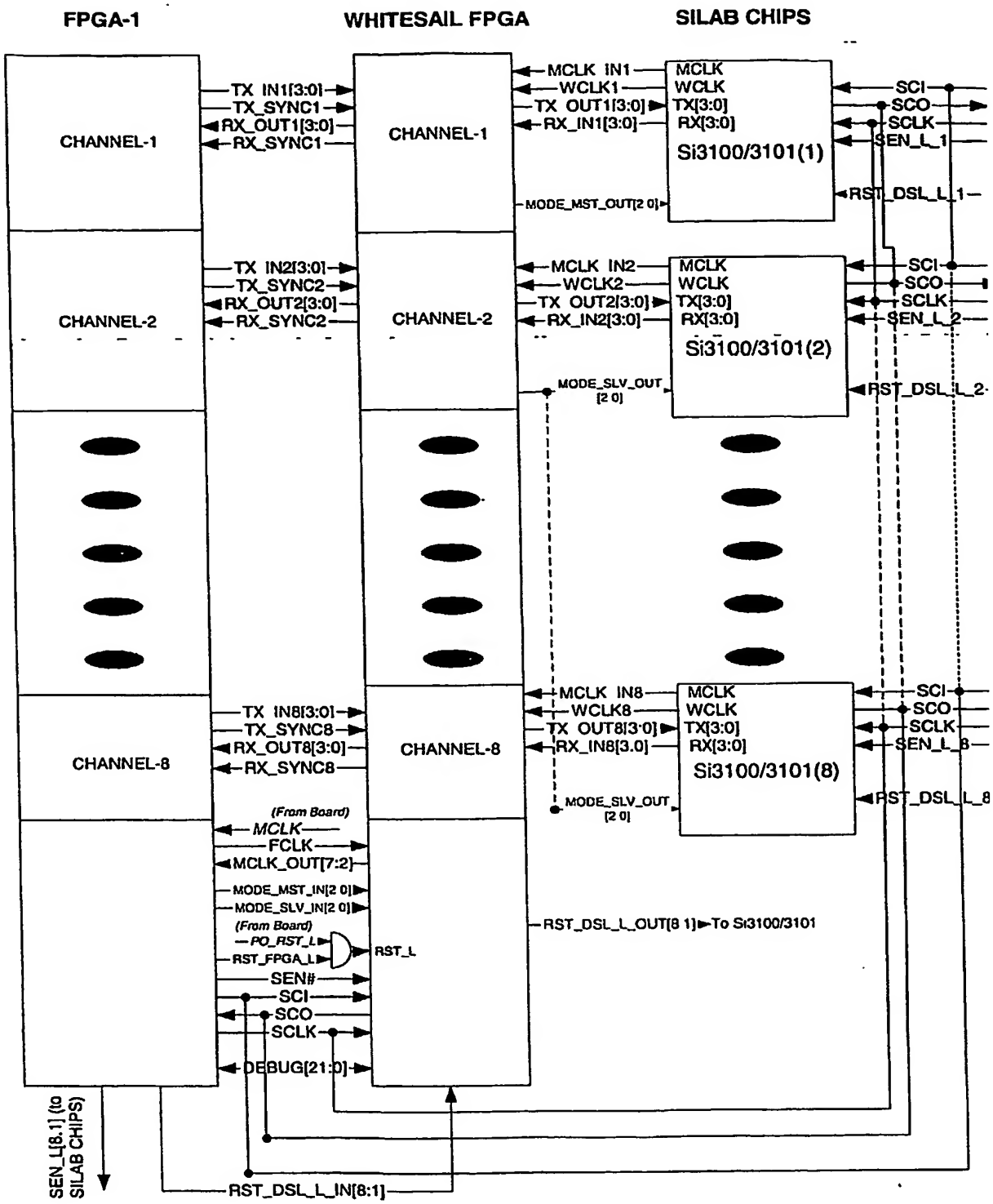
IS	IS NOT.
• Supports Nibble Data interface @35.328MHz from/to the SILAB (Si3100/Si3101) chips • Supports Nibble Data interface @35.328 MHz from/to FPGA-1 • Up-samples and does a LPF on the data coming from FPGA-1 (TX-Filter) • Does a LPF and Down-samples data coming from the SILAB chips (RX-Filter) • Interfaces to Eight SILAB chips and has 8 corresponding pairs of RX & TX Filters • Supports a Serial Interface @ 8.832 MHz from FPGA-1 for register read/writes • A feed-through (from FPGA-1 to the SILAB chips) for the MODE inputs of the SILAB chips • A feed-through (from FPGA-1 to the SILAB chips) for the Reset inputs of the SILAB chips • < 1W of power • < 250 pins • XILINX VIRTEX-II XC2V1000 –5 FPGA • BG575 Package	• Serial/Control Interface to the SILAB chips • Reset Control of the SILAB chips • Control for the Mode inputs to the SILAB chips

2 Functional Description

The WHITESAIL FPGA provides the following functionality

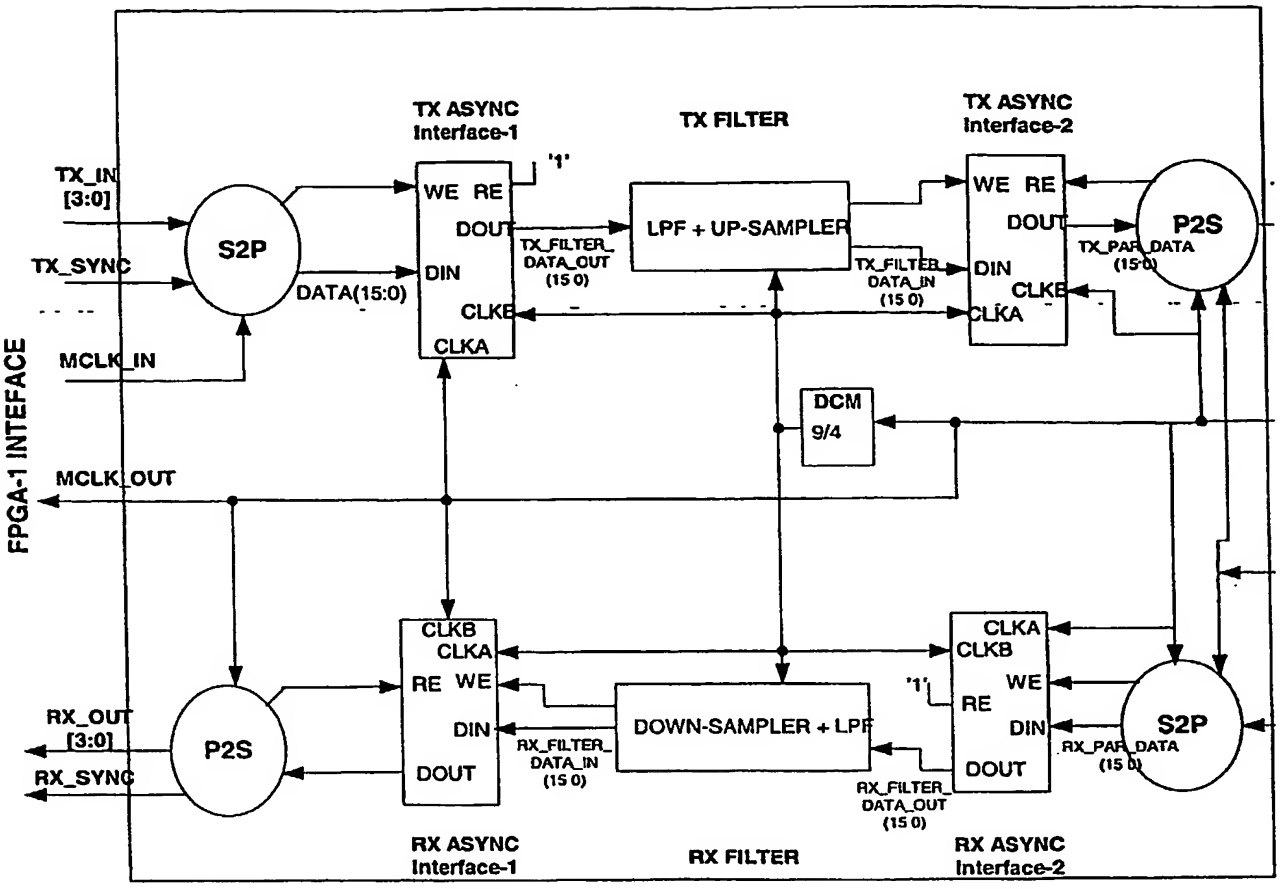
- Performs Serial to Parallel (S2P) conversion of the nibble data coming from the SILAB chips (Si3100/3101) and feeds it to the RX-Filter (LPF + Down-Sampler)
- Performs Parallel to Serial (P2S) conversion of the data from the RX-Filter and sends it to FPGA-1
- Performs Serial to Parallel (S2P) conversion of the nibble data coming from FPGA-1 and feeds it to the TX-Filter (Up-Sampler + LPF)
- Performs Parallel to Serial (P2S) conversion of the data from the TX-Filter and sends it to the SILAB chips

2.1 Interface Diagram



WHITESAIL FPGA Interface Diagram

2.2 Block Diagram



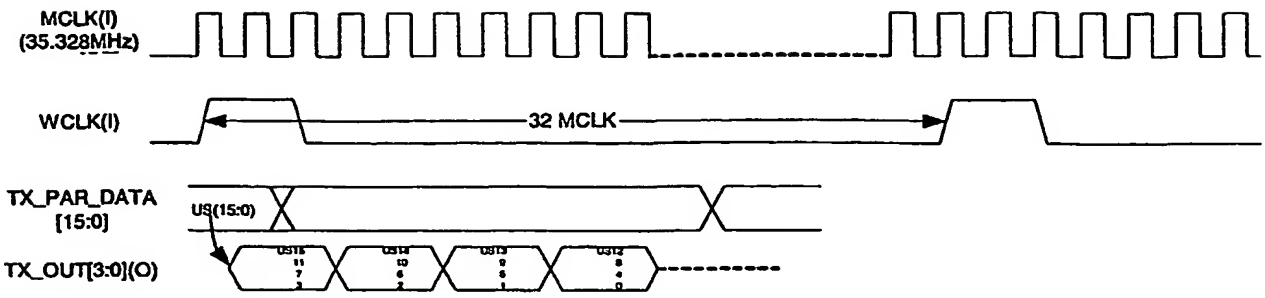
SINGLE CHANNEL BLOCK DIAGRAM

2.3 Parallel to Serial Converter (P2SC)

The parallel-to-serial converter takes the16-bit wide data and converts it into 4 nibbles (nibble = 4bits). The P2SC on the Si3100/3101 interface is slightly different than the P2SC on the FPGA-1 interface.

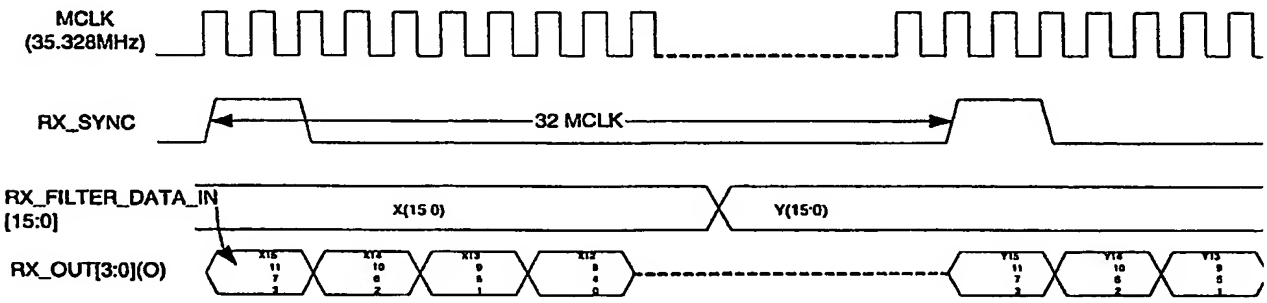
The P2SC on the Si3100/3101 interface is initiated when WCLK is asserted. 16-bits of data are read from the TX ASYNC FIFO-2 every 8 clocks by the P2SC. At steady state this interface bandwidth is 70.656Mbps (a nibble every 2 MCLK's).

The timing diagram for this interface is given below



The P2SC on the FPGA-1 interface is initiated whenever the RX ASYNC FIFO-1 is not empty. The RX Filter will write 16-bits of parallel data to this FIFO once every 32 clocks and thus interface bandwidth is 17.664Mbps.

The timing diagram for this interface is given below.

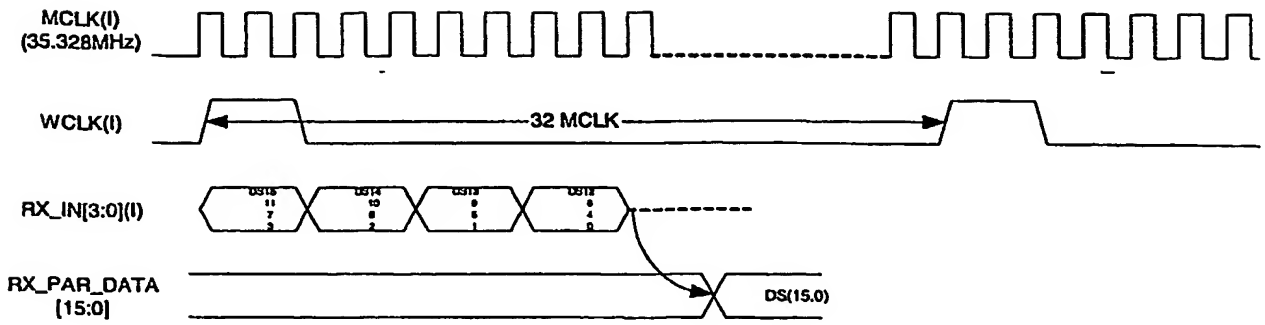


2.4 Serial to Parallel Converter (S2P)

The Serial-to-Parallel converter (S2PC) does exactly the reverse of what the P2SC does. The S2PC takes 4 nibbles of data from one interface and writes 16-bit parallel data to the other interface. The S2PC on the FPGA-1 interface and the Si3100/3101 interface differ slightly.

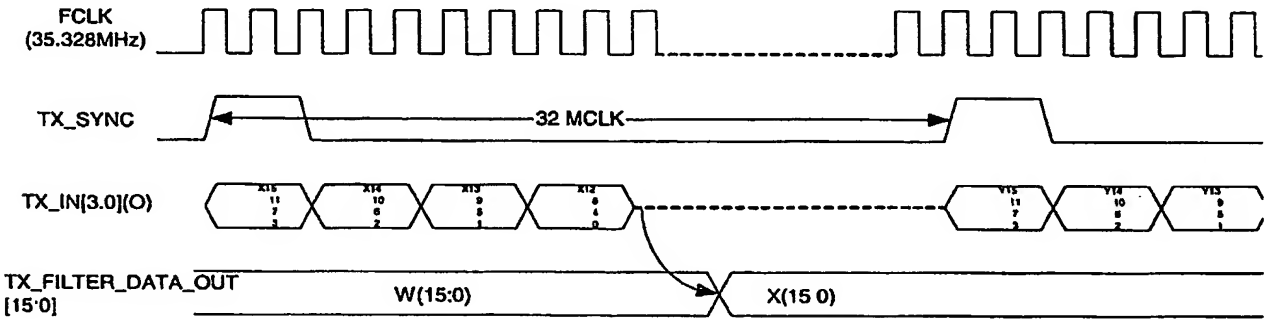
The S2PC at the Si3100/3101 interface is initiated when WCLK is asserted. A nibble of data is received from Si3100/3101 every 2 MCLK. The S2PC converts 4 nibbles of data to 16-bit parallel data and writes it to RX ASYNC FIFO-2. This interface bandwidth is 70.656Mbps (4 nibbles every 8 MCLK).

The timing diagram for this interface is given below



The S2PC at the FPGA-1 interface is initiated when TX_SYNC is asserted. The TX_SYNC signal is asserted once every 32 FCLK. The S2PC converts 4 nibbles of serial data to 16-bits of parallel data and writes it to the TX ASYNC FIFO-1. This interface bandwidth is 17.664Mbps (4 nibbles every 32 FCLK).

The timing diagram for this interface is given below



2.5 TX Filter

2.6 RX Filter

2.7 Serial Interface

This interface is used to read/write registers inside the WHITESAIL FPGA. The serial interface has 4 signals, SCLK (I), SCI (I), SCO (O) and SEN#(I). SCLK, SCI and SCO are shared by the WHITESAIL-FPGA and the 8 SILAB chips. However each of these slave targets has its individual enable (SEN#). The slave target will drive SCO only when a read cycle is issued by FPGA-1 to that particular target else it is tri-stated.

The timing diagram for the serial transfer is as shown below

ADD FIG.

2.8 Clocking

2.8.1 Data Path

The WHITESAIL FPGA gets 8 clocks from 8 different SILAB chips. All of these clocks (MCLK_IN [7:0]) have a fixed frequency of 35.328 MHz. These clocks are used by the 8 P2SC and S2PC pairs at the Si3100/3101 interface respectively.

The master MCLK (coming from Si3100/3101 number-0) is multiplied by a factor of 9/4 in the FPGA DCM. This clock is used by ALL of the TX/RX filters.

The P2SC at the FPGA-1 interface uses the master MCLK (MCLK_IN0).

The S2PC at the FPGA-1 interface uses FCLK (coming from FPGA-1).

2.8.2 Control Path

The control path in the WHITESAIL FPGA is clocked by SCLK, coming from FPGA-1. This clocks frequency is 8.832 MHz.

2.9 Power Up, Reset, and Configuration

2.9.1 Power Up

2.9.2 Reset

The WHITESAIL FPGA has the following resets

- Global Hard Reset (RST_L): This signal is generated by ANDing the power-on-reset (PO_RST_L), generated by the WHITESAIL board and the FPGA reset (FPGA_RST_L), generated by FPGA-1.
- Global Soft Reset (SRST): This reset is issued by software when it writes to the ??? register.
- Channel Resets (RST_DSL_L [7:0]): These are individual channel resets.

2.9.3 Configuration

The WHITESAIL FPGA is configured, using JTAG by the EPROM on the WHITESAIL board. The DONE signal of the FPGA will be connected to a LED on the board to indicate if the FPGA has been programmed successfully or not.

3 Programming Model

3.1 Register Map

The WHITESAIL FPGA address space is 128 Bytes (7 bits). All accesses are 16 bits.

Starting Address	Size	Segment Name	Data Direction	Description
0x00	128 Bytes	GLOBAL Segment	N/A	Revision, Mode, Global Space, Reset, etc.

WHITESAIL FPGA Register Map (all accesses 16-bits)			
Address	Page #	Name	Description
GLOBAL Segment			
0x00		FPGA_ID	FPGA ID Register
0x01		FPGA_REV	FPGA Revision Register
0x02		FPGA_SCRATCH	FPGA Scratch Pad Register
0x03-0x7F		*Reserved*	

3.2 Register Definitions

Each register is given a plain English name, as well as a unique identifier. Note that all addresses are always in hex.

Register bits may be labeled as read-only, read-write, or reserved. The default access is read-write unless otherwise noted.

- **Read-only (RO):** Reads will return the value of the register. Writes will be ignored.
- **Write-only(WO):** Only writes allowed. Read data should be ignored.
- **Read-Write (RW):** Both reads and writes are allowed.
- **Read and Clear (RC):** The register bits are reset whenever the software reads the register
- **Reserved:** Software should ignore anything read from these bits, and it is illegal to change the value of these bits. Changing the value of reserved bits will result in undefined operation.

Registers at reserved addresses must never be read or written. Unless otherwise stated, all of the registers are read/writeable.

3.2.1 GLOBAL Segment

FPGA ID Register (RO)															
FPGA_ID (0x00)															
15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
FPGA_ID (15:0)															

Name	Bit #	Description
FPGA_ID [15:0]	15:0	16-bit read-only value uniquely identifying the WHITESAIL FPGA. Default=0x?????

FPGA Revision Register (RO)															
FPGA_REV (0x01)															
15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
MajorRev								MinorRev							

Name	Bit #	Description
MinorRev[7:0]	7:0	8-bit BCD value indicating the minor revision of the chip. Default = 0x0
MajorRev[7:0]	15:8	8-bit BCD value indicating the major revision of the chip. Default = 0x0

16 bit Scratch Pad Register															
FPGA_SCRATCH (0x02)															
15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Scratch [15:0]															

Name	Bit #	Description
Scratch [15:0]	15:0	16-bit scratch register. Default = 0x0000

4 Pin List

All signals are LVTTL (3.3V) signaling levels unless otherwise noted.

Pin count summary:

FPGA-1 Interface:	93
Si3100/3101 Interface:	80
Reset, Test and Misc.:	43
Total	216

4.1 Interface timing

4.2 Signal List

4.2.1 FPGA-1 Interface (up to 35.328 MHz)

Signal Name	Location	Direction	Total	Signal Description
FCLK		I	1	Clock from FPGA-1
TX[7:0]_OUT[3:0]		I	32	TX Nibble Data (8 Channels)
TX_SYNC [7:0]		I	8	SYNC for the TX data (8 Channels)
RX[7:0]_OUT[3:0]		O	32	RX Nibble Data (8 Channels)
RX_SYNC [7:0]		O	8	SYNC for the RX data (8 Channels)
MCLK[7:2]_OUT		O	8	MCLK (Channels 2 to 8)
SCLK		I	1	Serial Interface Clock
SCI		I	1	Serial Data In
SCO		0	1	Serial Data Out
SEN_L		I	1	Serial Enable
		TOTAL:	93	

4.2.2 Si3100/3101 Interface (35.328 MHz)

Signal Name	Location	Direction	Total	Signal Description
MCLK[7:0]_IN		I	8	MCLK (8 Channels)
WCLK[7:0]		I	8	Frame Sync for Data transfer
TX[7:0]_IN[3:0]		O	32	TX Nibble Data (8 Channels)
RX[7:0]_IN[3:0]		I	32	RX Nibble Data (8 Channels)
		Total:	80	

4.2.3 Reset, Test and Misc. Signals

Signal Name	Location	Direction	Total	Signal Description
RST_L		I	1	Reset
RST_DSL_L [7:0]		I	8	Individual Resets for the 8 Channels
MODE_MST_IN [2:0]		I	3	SILAB Chips Mode
MODE_SLV_IN [2:0]		I	3	SILAB Chips Mode
MODE_MST_OUT [2:0]		O	3	SILAB Chips Mode
MODE_SLV_OUT [2:0]		O	3	SILAB Chips Mode
DEBUG [21:0]		I/O	22	Debug Signals
		Total:	43	

WhiteSail AFE Requirements

1. Purpose

This document identifies key requirements of the WhiteSail AFE design, and associated tests used to verify compliance to these requirements.

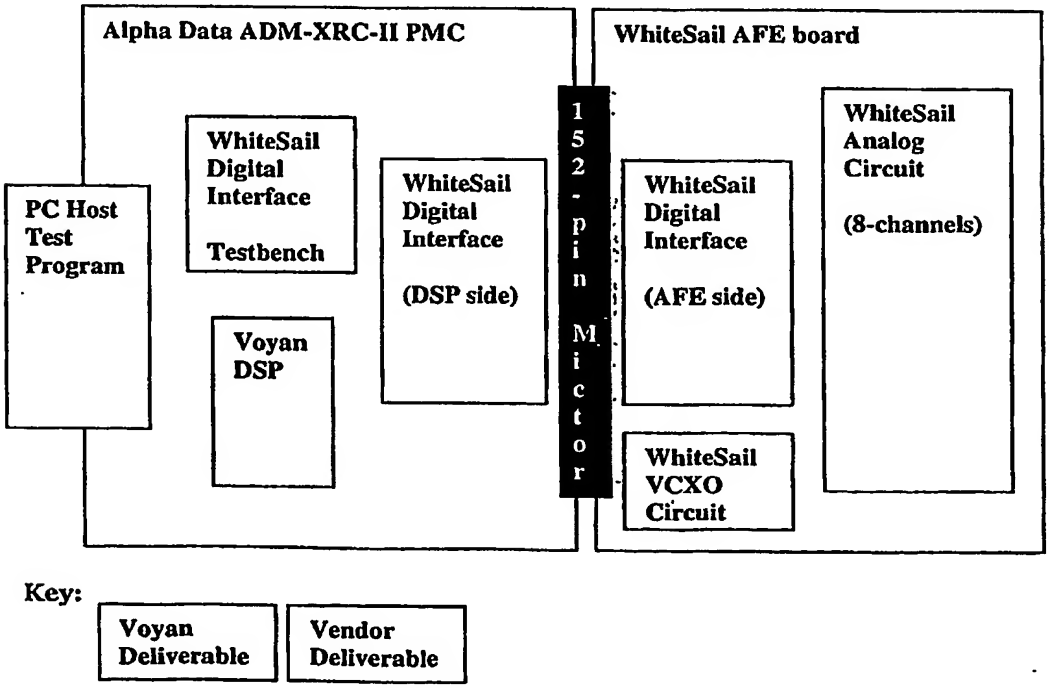
2. Assumptions

These assumptions have been made in this requirements document:

1) The Silicon Laboratories Si3101 AFE is used in the circuit.
2) Voyan's analog circuit design (transformer through Si3101) is incorporated in the design.
3) The WhiteSail board will interface through a 152 pin Mictor connector to an Alpha Data ADM-XRC-II PCI Mezzanine Card (PMC). Voyan's digital transceiver processing is resident on this board. The ADM-XRC-II product manual (including connector pinout) is included as an appendix to this document.
4) The WhiteSail board vendor is responsible for a detailed specification of the custom digital interface to the board. The WhiteSail digital interface is inclusive of:
   a) the board level circuitry on the digital side of the SiLabs AFE.
   b) the connector pinout and signal definition between the Alpha Data FPGA PMC.
   c) the VHDL interface module residing in the Alpha Data FPGA PMC.
5) The WhiteSail board vendor will provide a VHDL testbench for the board. When implemented on the Alpha Data PMC, this testbench will exercise all required operation modes of the AFE. Voyan will complement this testbench with a host-based program to send and receive test vectors to/from the WhiteSail board.
6) The maximum word clock rate to/from the AFE board is 1.104 MHz.

3. Block Diagram – Digital side

Figure 1 delineates the separation of responsibility between the vendor deliverables and what is developed by Voyan:



Voyan requires a register based interface to the AFE board, such that two 16-bit registers per channel (one Tx, one Rx) exists for the DSP to write/read to the AFE). A channel specific control port should exist to set/get AFE parameters. The WhiteSail board vendor has freedom to implement the actual interface in the most appropriate way, as long as the DSP access is via registers.

4. Detailed Block Diagram – Analog side

A detailed block diagram of the analog portion of the AFE board is shown in Figure 2. Only 1-channel of a total of 8 per board are shown in the block diagram:

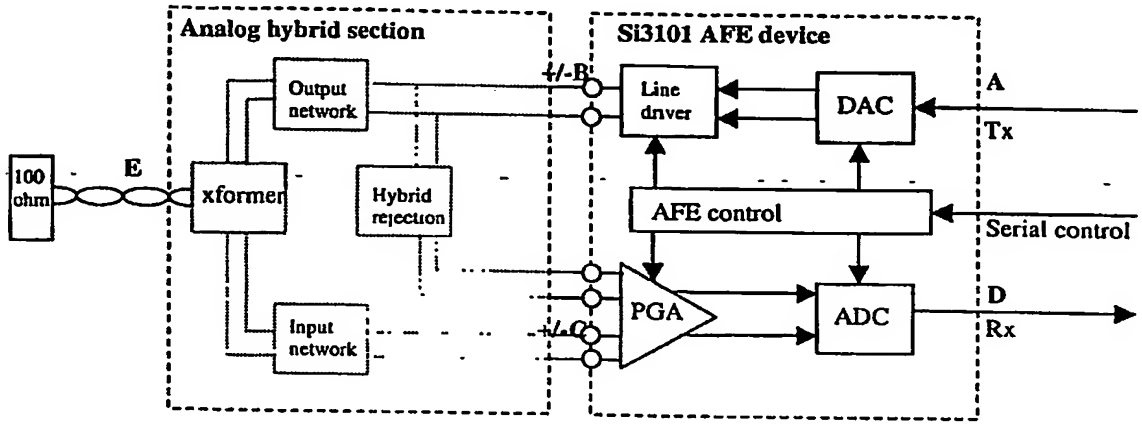


Figure 2. AFE block diagram and test points

5. Deliverables

The project deliverables from the WhiteSail board vendor to Voyan are listed as follows, in the order of their delivery:

1. ***AFE Digital Interface Specification*** – includes Mictor pinout and timing specification of the bank of registers that Voyan DSP writes/reads to access the AFE data.
2. ***AFE Digital Interface VHDL*** – for inclusion by Voyan into the logic of the AlphaData ADM-XRC-II FPGA.
3. ***AFE Digital Interface Testbench*** – for inclusion by Voyan into the logic of the AlphaData ADM-XRC-II FPGA. Subsequent Voyan development
4. ***WhiteSail AFE board schematic*** –
5. ***WhiteSail AFE board layout*** – Gerber files and artwork.
6. ***WhiteSail AFE board blanks*** – Quantity 8.
7. ***Loaded and tested WhiteSail AFE board*** – Quantity 8.
8. ***Custom cable to connect WhiteSail board to Alpha Data board*** – Quantity 8.

6. Specifications and Test Requirements

The following specifications assume use of the Silicon Laboratories Si3101 AFE. Those specifications related to the test of the WhiteSail board are included below:

Noise Dynamic Range

1. D must have input noise dynamic range < -90 dBFS, with A=0 (zero transmitter output).
2. B must have output noise dynamic range < -80 dBFS, with A=0.

THD

3. D must have THD < -85 dBFS, for A=0, F=1/4 power tone at 150 kHz.
4. B must have THD < -75 dBFS, for A=1/4 power tone at 150 kHz.

MTPR

5. D must have MTPR < -85 dB, for A=multi-tone test signal (supplied).
6. B must have MTPR < -75 dB, for A= multi-tone test signal (supplied).

Hybrid Rejection

7. C/B: -25 dB overall rejection (this can be tuned to the worst case loop (CSA #6) at 9000 feet)
Per Figure 3, the rejection as a function of frequency requirement is:

- −18 dB to −28 dB (linear slope in dB) from 10 kHz to 130 kHz
- −28 dB from 125 kHz to 400 kHz
- −28 dB to −18 dB (linear slope in dB) from 400 kHz to 550 kHz

For loops shorter than CSA6, the rejection requirement is lessened. For example, in Figure 3, the flat part of the rejection curve can be 6 dB higher (−22 dB) for CSA6-1 (7500 feet). For this case the rejection requirement is only −19 dB (aggregate over all frequencies).

Measurement #1:
A off, F on (broadband noise), measure the transfer function C/E. If measurement point C is not accessible, infer from the digital word at point D.

Measurement #2:
A on (broadband noise), F off, measure C/B.

The noise injected at A and F must be at the same level. Verify that Measurement #2 divided by Measurement #1 <= -25 dB, and further that the transfer function ratio conforms to the Figure 3 frequency requirement.

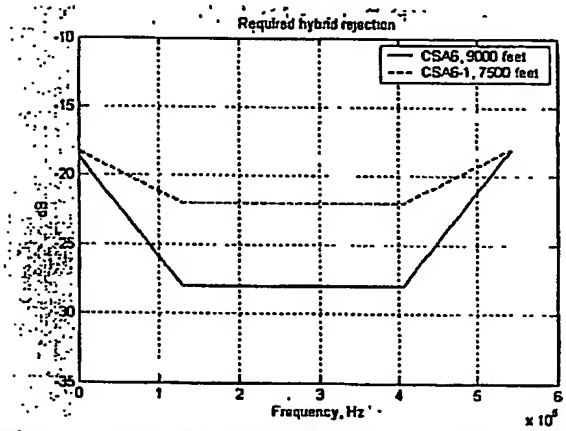


Figure 3. Overall hybrid rejection of −25 dB, stated as a function of frequency, per specification 5.8. Loops other than CSA6 have reduced requirements.

7. DAC-driven VCXO

The maximum sample rate of the system is 1.104 MHz, and is the same for the DAC and ADC. A VCXO clock is required either on the device or the AFE board, that has these characteristics:

1. The VCXO circuit should present a register based interface from the FPGA that allows Voyan to implement clock recovery and tracking in software.
2. The maximum VCXO update rate is specified at 8192 Hz.
3. VCXO frequency stability (maximum deviation from nominal frequency) = 25 ppm.
4. The VCXO should be tunable via a 12-bit DAC over a frequency range of +/− 50 ppm from the nominal clock frequency.
5. VCXO clock jitter should be less than -85 dBc at 10 Hz away from the VCXO nominal frequency.

This document describes the functional specifications for the Voyan OptiFusion line card called *White Sail.*

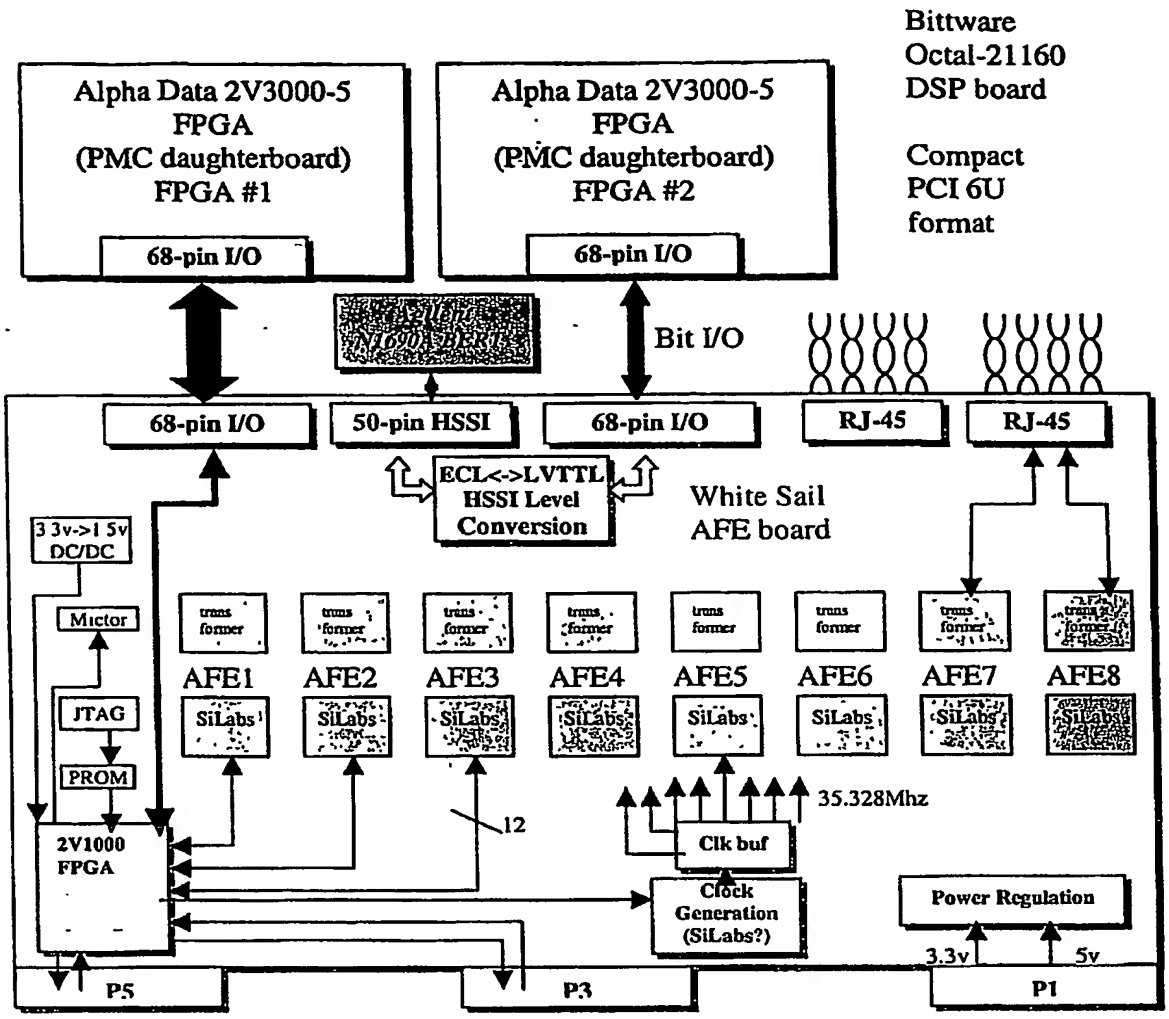


Figure 1 - Block Diagram

Clocking:

We need all of the AFE chips to be synchronized if we do not want to build a synchronizer into the receiving chip. To do this, we need to disable the internal VCXO and derive the clock externally. The internal VCXO has a step size of between 0.03 and 0.34 ppm, depending on where it is in the range.

Questions:

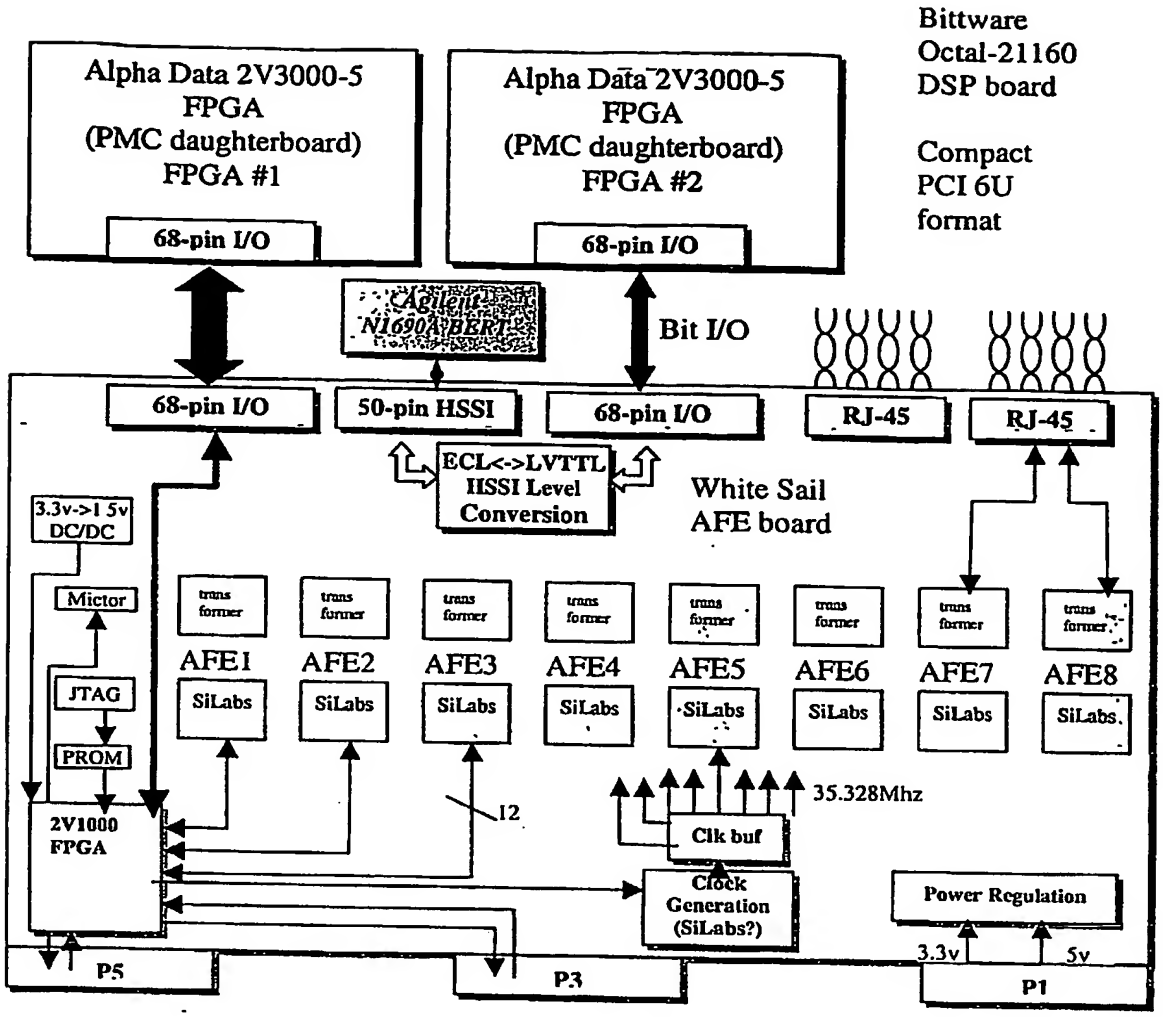
- Does the SCLK have to be exactly 4x the MCLK? Or is there an internal synchronizer?
- What is the delay from XIN to MCLK out?
- The clock variation is to accommodate variations in the CO's DSL clock. If all of the AFEs are running off the same clock, that assumes that all of the inputs are from one CO. Is this a valid assumption?

HSSI Interface

The HSSI interface is driven at ECL levels to a 50pin high density connector with the following pinout:

Signal Name	Dir.	Pin # (+side)	Pin # (-side)
SG - Signal Ground	---	1	26
RT - Receive Timing	<--	2	27
CA - DCE Available	<--	3	28
RD - Receive Data	<--	4	29
- reserved	<--	5	30
ST - Send Timing	<--	6	31
SG - Signal Ground	---	7	32
TA - DTE Available	-->	8	33
TT - Terminal Timing	-->	9	34
LA - Loopback circuit A	-->	10	35
SD - Send Data	-->	11	36
LB - Loopback circuit B	-->	12	37
SG - Signal Ground	---	13	38
5 ancillary to DCE	-->	14 - 18	39 - 43
SG - Signal Ground	---	19	44
5 ancillary from DCE	<--	20 - 24	45 - 49
SG - Signal Ground	---	25	50

Pin pairs 5&30, 14&39 to 18&43, and 20&45 to 24&49 are reserved for future use. To allow future backward compatibility, no signals or receivers of any kind should be connected to these pins.


Alpha Data 2V3000-5
FPGA
(PMC daughterboard)
FPGA #1
68-pin I/O
Alpha Data 2V3000-5
FPGA
(PMC daughterboard)
FPGA #2
68-pin I/O
Bittware
Octal-21160
DSP board
Compact
PCI 6U
format
Agilent
N1690A BERT
Bit I/O
68-pin I/O
50-pin HSSI
68-pin I/O
RJ-45
RJ-45
ECL<->LVTTL
HSSI Level
Conversion
White Sail
AFE board
3.3v->1.5v
DC/DC
Mictor
JTAG
PROM
2V1000
FPGA
trans former
AFE1
AFE2
AFE3
AFE4
AFE5
AFE6
AFE7
AFE8
SiLabs
12
35.328Mhz
Clk buf
Clock
Generation
(SiLabs?)
Power Regulation
3.3v
5v
P5
P3
P1

White Sail
Functional Specification

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- IEEE 1011.11
- IEEE 1149.1
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- Wave Functional Specification
- White Sail Layout Guidelines
- White Sail Schematics

1.2 Scope

The purpose of this document is to present the high-level design aspects of the White Sail board. The reader should refer to the schematics for the actual implementation of the concepts presented in this document.

1.3 Overview

The White Sail board is part of a communications system based on DSL technology. The design utilizes eight synchronized, DSL channels to transport aggregated data for the system. Part of the data aggregation and data processing is performed on board using an FPGA, code-named Wave. The Wave chip then transports the data to the system where data is handled by other elements.

The design primarily uses 3.3V and 5.0V to power the circuitry. The voltage rails are provided by the power subsystem in a CompactPCI chassis or through an external power supply if the board is in stand-alone operation. In either case, the data interface to the system consists of a high-speed ribbon cable.

2 Design Specification and Implementation

2.1 Design Objectives

The design is based on the Silicon Labs' DSL ASIC, Si3101-KQ, and the respective evaluation platform. The following is a list of the objectives:

- Conform to the specifications for a CompactPCI 6U, rear I/O form factor
- Provide eight DSL channels, where one is master and seven are slaves
- Synchronize each slave channel to the master channel
- Hot swap capable at the hardware level
- Provide for two sources of power and condition the rails accordingly
- Provide test features such as logic analyzer taps, test points, and visual indicators
- Incorporate an FPGA and its supporting circuitry for data processing and control
- Use a reset strategy based on power-up sequencing which then relinquishes control to the system reset inputs
- Design the board to be backwards compatible with Si3100-KQ (Rev C) AFE's

The following is a list of design considerations that shall not be incorporated:

- Hot swap capable at the software level

- Meets all compliance standards for safety
- Designed for surge immunity, i.e. lightning strikes, wet line shorts, etc.
- Provide for an alternate data path to the system in essence bypassing Wave

2.2 Block Diagram

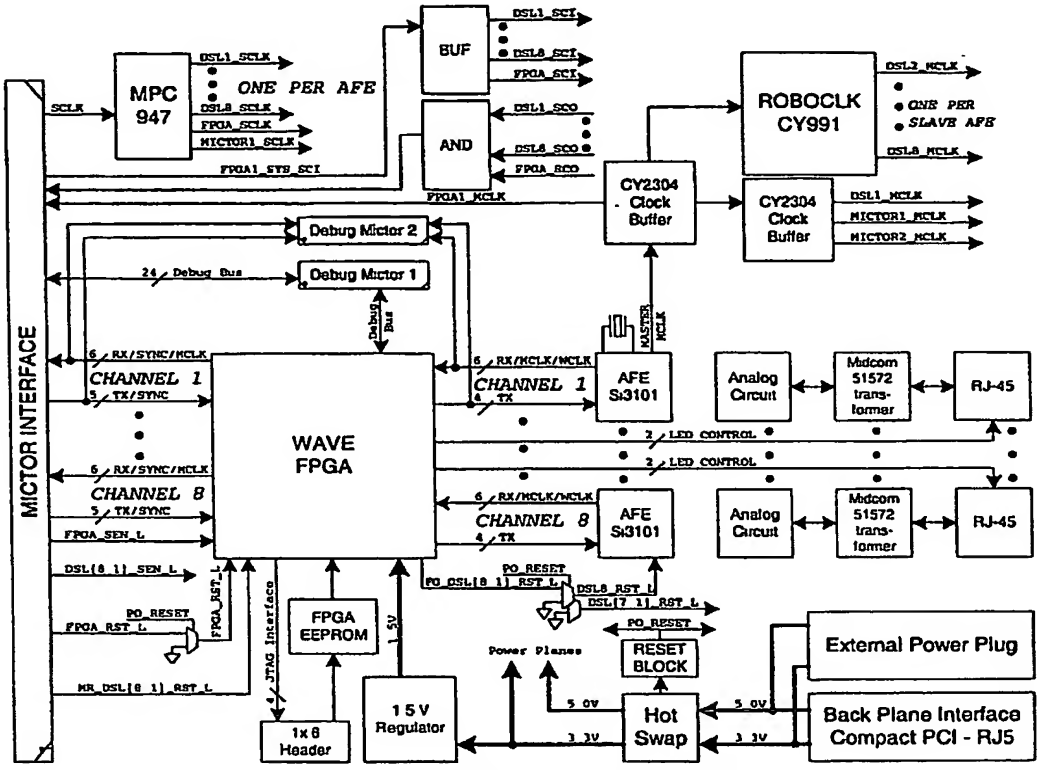


Figure 2-1: White Sail Block Diagram

2.3 Power and Hot Swap

As shown in the block diagram, power originates from one of two sources, either the back plane in a CompactPCI chassis or from external power supplies connected through the external power plug on the board. These voltage rails, 3.3V and 5.0V, feed through a hot swap controller to carefully ramp the rails for the rest of the circuitry. There is also a voltage regulator that uses the 3.3V rail as a source of power to generate the 1.5V rail used by Wave.

The hot swap controller monitors the primary rails, 3.3V and 5V, for under-voltage and short-circuit conditions. The design also uses independent, precision voltage monitors for each of the three voltage rails. The monitors and the hot swap controller tie into the reset circuitry.

2.4 Clock Distribution

2.4.1 Nibble Interface (MCLK)

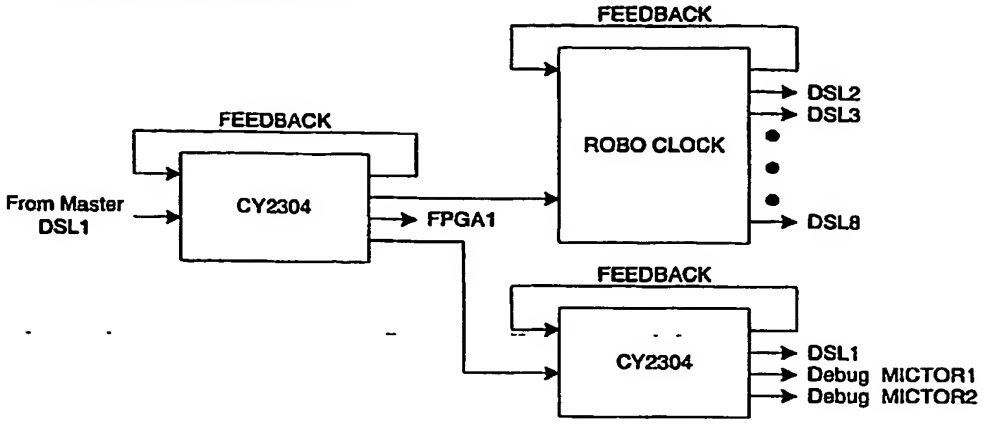
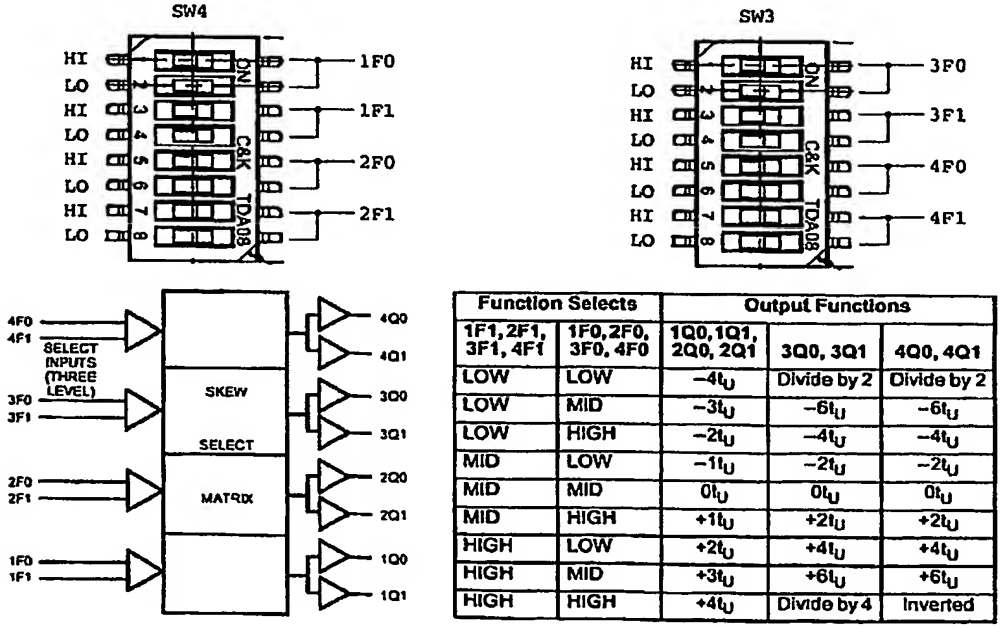


Figure 2-2: MCLK Distribution

The primary channel (DSL1) is the root for all other devices on the board. DSL1 uses an external crystal with its internal VCXO to generate the MCLK signal for the nibble interface. A copy of the MCLK output is used to fan out the clock inputs to the other DSL channels through a series of zero delay buffers. The goal is to minimize skew and jitter while providing a synchronous clock to all devices.

For the purposes of debug or fine tuning, the clock inputs to the slave channels may be skewed with respect to the clock for the master channel. This is accomplished by manipulating control switches that are connected to the ROBO clock device. Note that the skews introduced by these controls are not symmetric across all outputs.



Function Selects		Output Functions		
1F1, 2F1, 3F1, 4F1	1F0, 2F0, 3F0, 4F0	1Q0, 1Q1, 2Q0, 2Q1	3Q0, 3Q1	4Q0, 4Q1
LOW	LOW	$-4t_U$	Divide by 2	Divide by 2
LOW	MID	$-3t_U$	$-6t_U$	$-6t_U$
LOW	HIGH	$-2t_U$	$-4t_U$	$-4t_U$
MID	LOW	$-1t_U$	$-2t_U$	$-2t_U$
MID	MID	$0t_U$	$0t_U$	$0t_U$
MID	HIGH	$+1t_U$	$+2t_U$	$+2t_U$
HIGH	LOW	$+2t_U$	$+4t_U$	$+4t_U$
HIGH	MID	$+3t_U$	$+6t_U$	$+6t_U$
HIGH	HIGH	$+4t_U$	Divide by 4	Inverted

Figure 2-3: ROBO Clock Skew Control

2.4.2 Serial Interface (SCLK)

The clock for the serial interface to all Silicon Laboratories chips originates from FPGA1 in the main system. This signal is buffered on the board using a Motorola one to nine, fan-out buffer with a non-zero delay of approximately nine nanoseconds. Therefore each device receives a single ended copy of the original SCLK signal except for the FPGA, which shares its input with a debug Mictor™ connector.

2.4.3 JTAG Interface (TCK)

The JTAG clock is used for the programming of the serial EEPROM and the FPGA. The clock originates from the Xilinx programmer and is buffered on the White Sail board. The general-purpose buffer is used to create a single ended duplicate of the original signal.

2.5 Reset Strategy

Once the 3.3V and 5V voltage levels have reached their appropriate thresholds, the hot swap controller releases its reset signal to the reset block. The reset block consists of three voltage monitors or sensors and some reset logic. Each sensor along with the hot swap controller asserts an independent signal that gates the power-on reset signal. Once the respective voltage level is reached, the monitor delays the release of power-on reset for 150ms. The power-on reset signal shall assert if any of the voltage rails fail to achieve or maintain their appropriate level. The power-on reset signal can also be asserted manually via the push-button signal feeding the hot swap controller.

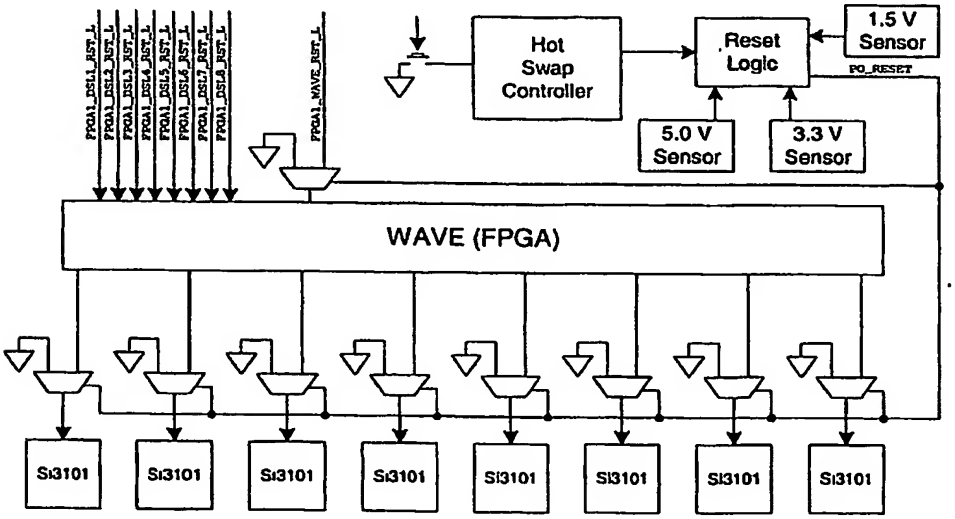


Figure 2-4: Reset Distribution

2.6 WAVE

Wave is an FPGA designed to manage the data between the eight DSL channels and the main system.

2.7 External Interfaces

2.7.1 DSL Channel Connectors

Each DSL channel employs a single RJ-45 style connector with dual integrated light emitting diodes. Only pins 5 and 7 are used as the line side interface to the user. Note that this connector does not provide sufficient protection against high potential conditions such as a lightning strike. Based on the product specification this design limitation was deemed acceptable and thus for convenience this connector is employed.

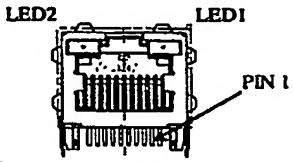


Figure 2-5: DSL Interface

2.7.2 Power Interface

The board shall provide a means of applying external power when not plugged into the chassis. This is accomplished through the use of a two by two header (4 pin) that is keyed to avoid incorrect insertion. The mating plug houses the crimped pins that connect to wires leading to the external power supply. This wire assembly shall serve as the power harness as shown in the following diagram.

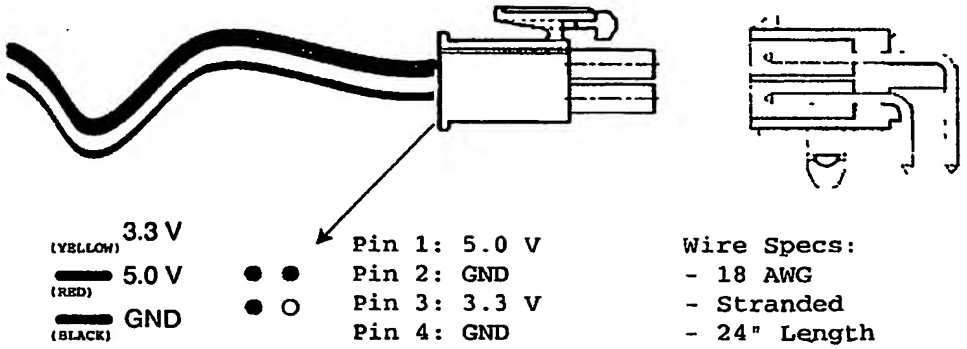


Figure 2-6: Power Harness Assembly

2.7.3 Front Panel Switches

2.7.4 LED Indicators

2.7.4.1 Front Panel Indicators

The front panel shall have a single light emitting diode to indicate the condition of the power subsystem, where ON (green) denotes a "power good" condition and OFF indicates a problem with the power subsystem.

Each DSL channel shall have a minimum of two light emitting diodes with the ability to support up to four light emitting diodes. These diodes are controlled directly by the WAVE chip with no buffering mechanism on the board. This implies that the appropriate drivers should be chosen for the WAVE chip to handle the drive requirements of the diodes. The operating current may range anywhere between 5.5mA to 7.5mA. The recommended drivers for these diodes are LVTTL24.

The following tables serve as truth tables for controlling the light emitting diodes under each available option. The columns LEDxA and LEDxB represent the driving signals from the FPGA, where x represents either LED 1 or LED 2 for a given DSL channel.

LEDxA	LEDxB	State
LO	LO	Off
LO	HI	Green/Yellow[1]
HI	LO	Off
HI	HI	Off

Figure 2-7: Functional behavior for LED on 406549-1

LEDxA	LEDxB	State
LO	LO	Off
LO	HI	Green
HI	LO	Orange
HI	HI	Off

Figure 2-8: Functional behavior for LED on 406549-7

2.7.4.2 Board Level Indicators

The design shall incorporate light emitting diodes to indicate board level events that are useful in a laboratory bring-up environment. The following table highlights the LED indicators that are included in the design.

Label	State Description		Color
	ON	OFF	
DONE	FPGA programming completed	FPGA is not programmed	Green
PWR_RST	Reset is asserted due to user interrupt or voltage rail outside the specified range	All voltage rails are within the specified range	Red
PWR_GOOD	All voltage rails are within the specified range	Reset is asserted due to user interrupt or voltage rail outside the specified range	Green[2]
5.0V	5.0V rail is enabled through the hot swap controller	Hot swap controller has not released the 5.0V rail	Green
3.0V	3.3V rail is enabled through the hot swap controller	Hot swap controller has not released the 3.3V rail	Green

Figure 2-9: Board level LED descriptions

[1] LED1 is green while LED2 is yellow, refer to figure 2-2 for relative positions on the RJ-45 connector
[2] This LED is visible through the front panel as stated in section 2.7.4.1

3 Mechanical

3.1 Board Fabrication Information

3.1.1 Physical Dimensions

The board's form factor shall conform to the CompactPCI specification for a 6U, rear I/O card. The mechanical drawings can be found in the CompactPCI specification, PICMG 2.0 R3.0 that is also governed by IEEE specifications 1011.1, 1011.10, and 1011.11.

3.1.2 Stack-Up

Board Thick	#		CU oz	Dielect.	Comments
S	1		0.6		.0065 traces=50.8ohms or .005 traces=57.6
I		PREPREG		4	
P	2		0.6		
I		CORE		5	
S	3		0.6		.004 traces = 49 ohms
I		PREPREG		5	
P	4		0.6		
I		CORE		5	
P	5		0.6		
I		PREPREG		5	
S	6		0.6		.004 traces = 49 ohms
I		CORE		5	
P	7		0.6		
I		PREPREG		5	
S	8		0.6		.004 traces = 49 ohms
I		CORE		5	
P	9		0.6		
I		PREPREG		5	
S	10		0.6		.004 traces = 49 ohms
I		CORE		5	
P	11		0.6		
I		PREPREG		4	
S	12		0.6		.0065 traces=50.8ohms or .005 traces=57.6
TOTAL LAMINATION THICKNESS:			7.20	53	Total thickness .062

Table 3-1: Board Construction (Stack-up)

3.2 Placement

The following diagram highlights the placement of key functional blocks in the design. The diagram is not to scale, although the diagram was extracted from the manufacturing CAD tools.

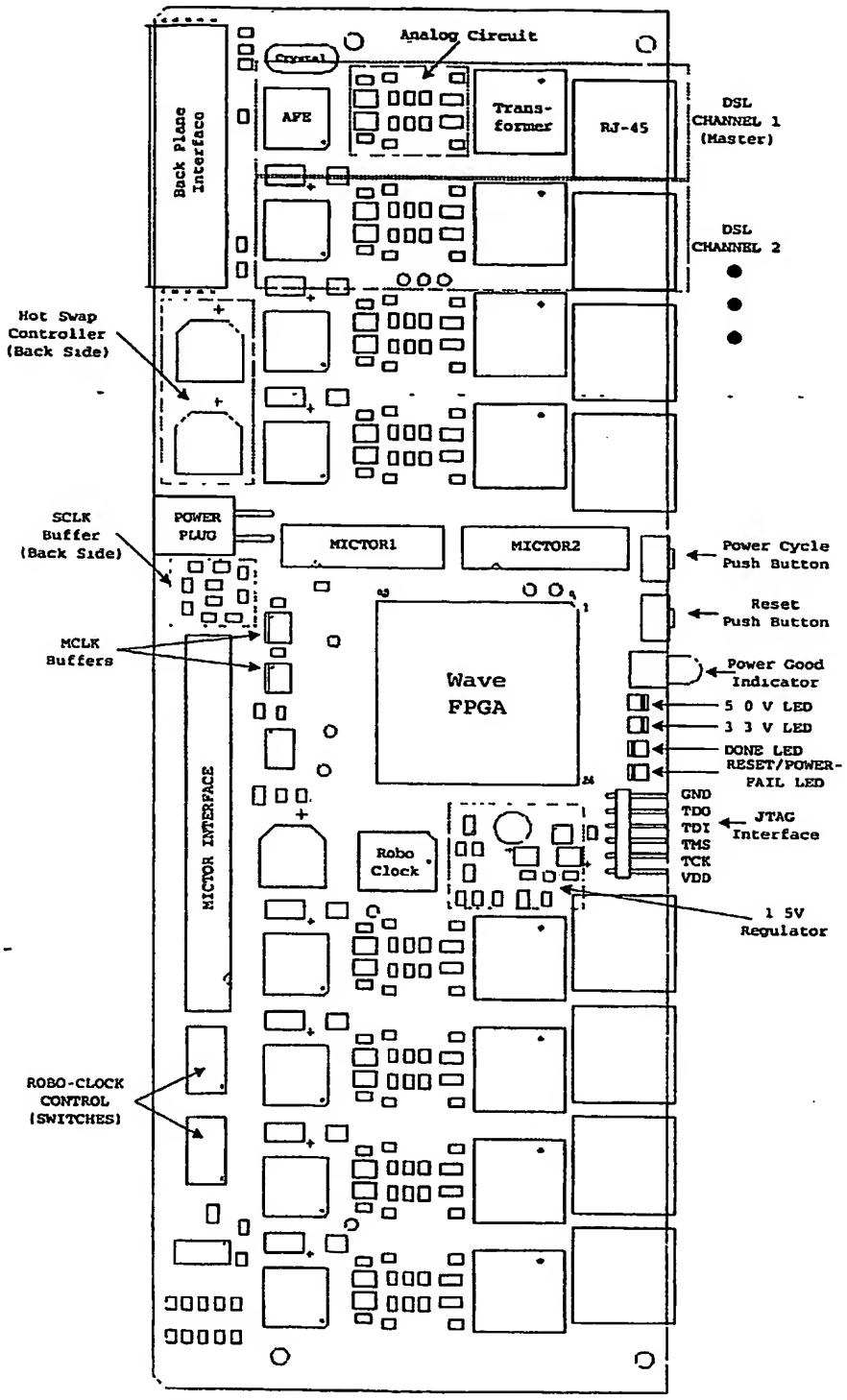


Figure 3-1: Component Locations Highlighting Key Devices

3.3 Front Panel

The front panel features openings for each of the eight DSL channels. The "power good" indicator should be visible from a 120 degree viewing angle. There are also two small openings to access the "power cycle" and "reset" switches using a small poking implement, such as a plastic stylus. The front panel also features two ergonomic, latching handles, which facilitate insertion and/or extraction from the chassis.

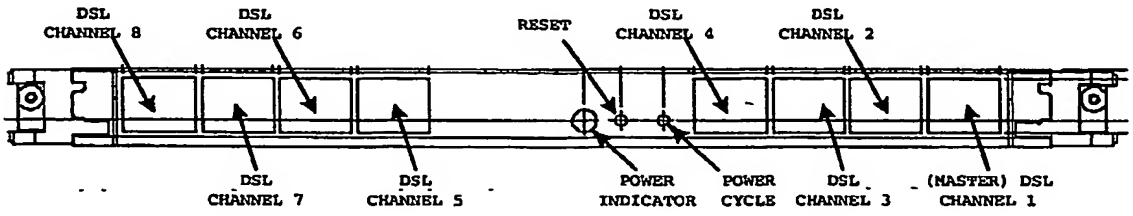


Figure 3-2: Front Panel Cut Outs

4 Electrical

4.1 Timing Information

4.1.1 Wave – AFE Interface (a.k.a. Nibble Interface)

The nibble interface should adhere to the timing diagrams specified in the Si3101-KQ (AFE) data sheet. There is not enough timing margin to perform transactions on a single clock edge based on the "hold" requirements specified in the data sheet.

4.1.2 Wave/FPGA1 Interface (Mictor™ Interface)

The interface between the main system and the White Sail board shall consist of a high-speed cable assembly. This cable assembly is a significant variable when determining the timing budget between the FPGA devices on each end of the cable interface. Based on the timing diagram that follows, the recommended cable length is thirty inches.

The signals F1_WV_TX and WV_F1_RX represent the data busses, which go between FPGA1 in the system and WAVE on the White Sail board. The signal F1_WV_TX represents the data passing from FGPA1 to WAVE while WV_F1_RX represents the data passing from WAVE to FPGA1.

The large skew between FPGA1_MCLK and WAVE_MCLK is largely attributed to the propagation delay across the cable, where both clocks originate on the White Sail board yet FPGA1 must receive its clock across the cable.

Row		Name	Formula	Min	Max	Margin	Comment
1	V	CableLen	30	30	30		Cable length
2	V	CableTpd	([min(CableLen),max(CableLen)]*0.16)	4.8	4.8		Propagation delay
3	V	TraceDiff	[5,]	5			Difference in clock lengths
4	V	TraceTpd	[(TraceDiff*0.18),]	0.9			Propagation delay
5	V	Clk2out	[0.69,2.99]	0.69	2.99		FPGA clock to out
6	D	DelayTot	[min(((Clk2out+BusTpd)+CableTpd)),max(((Clk2out+BusTpd)+CableTpd))]	5.85	8.69		Total drive delay
7	V	BusLen	[2,5]	2	5		Bus trace lengths
8	V	BusTpd	([min(BusLen),max(BusLen)]*0.18)	0.36	0.9		On board propagation delay
9	C	Setup	[3.61,]	3.61		<11.81,	FPGA Setup time
10	C	Hold	[(-2.28),]	-2.28		<8.13,	FPGA Hold time
11	D	WV_TpdTot	[min(((Clk2out+BusTpd)+CableTpd)),max(((Clk2out+BusTpd)+CableTpd))]	5.85	8.69		Total drive delay
12	C	F1_Setup	[3.61,]	3.61		<19.61,	FPGA Setup time
13	D	DelayTot	[min(((Clk2out+BusTpd)+CableTpd)),max(((Clk2out+BusTpd)+CableTpd))]	5.85	8.69		Total drive delay
14	C	WV_hold	[(-2.28),]	2.20		<4.22,	FPGA Hold time

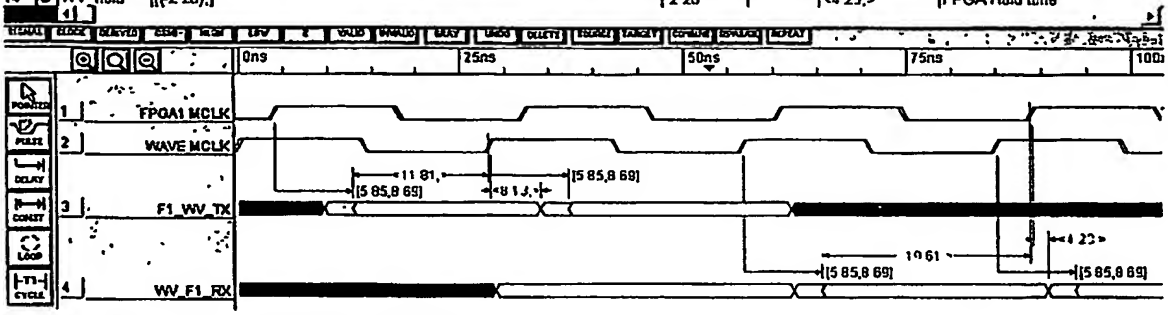


Figure 4-1: Timing Analysis for the Mictor Cable Assembly

4.1.3 Power Estimates

Power Estimates (based on MAX ratings)							
		Voltage Rail (V)					
		1.5		3.3		5	
Device	QTY	Imax (A)	Total	Imax (A)	Total	Imax (A)	Total
RoboClock Core	1	-	N/A	0.095	0.095	-	N/A
RoboClock Output Pair	4	-	N/A	0.019	0.076	-	N/A
RoboClock Biasing	8	-	N/A	0.009	0.072	-	N/A
Si3101	8	-	N/A	0.11	0.88	0.4	3.2
MPC947 core	1	-	N/A	0.028	0.028	-	N/A
MPC947 outputs	9	-	N/A	0.01	0.09	-	N/A
XC2V1000 quiescent	1	0.075	0.075	0.085	0.085	-	N/A
XC2V1000 core	1	0.4	0.4	-	N/A	-	N/A
XC2V1000 output	1	-	N/A	0.015	0.015	-	N/A
XC2V1000 aux	1	-	N/A	0.005	0.005	-	N/A
XC18V04	1	-	N/A	0.025	0.025	-	N/A
CY2304 Core	1	-	N/A	0.018	0.018	-	N/A
CY2304 Output	4	-	N/A	0.004	0.016	-	N/A
Power Regulator	1	-	N/A	-	N/A	0.25	0.25
HotSwap	1	-	N/A	-	N/A	0.025	0.025
Totals (A)			0.475		1.405		3.475
Power Dissipation (W)			0.7125		4.6365		17.375

Table 4-1: 5.0V, 3.3V, and 1.5V Power Estimates

4.1.4 Clock Distribution Skews and Jitter

Based on discussions with the technical staff, the design may tolerate a reasonable amount of skew (on the order of several nanoseconds) and less than 900ps of jitter. This is made possible by the correction algorithms that are used to recover and maintain clock synchronization with respect to the master DSL channel in the system. The following table highlights the component specifications that are outlined in the respective data sheets.

Device	Part to Part Skew	Output to Output Skew	Jitter
ROBO Clock	1.2ns	250ps	200ps
Cy2304	500ps	200ps	180ps
Si3101-KQ	Not Applicable	Not Applicable	Negligible

Table 4-2: Device Skew and Jitter Specifications

Assuming that jitter is cumulative and that the devices are operating at opposite extremes, the worst-case condition for the slave DSL channels with respect to the master channel is a clock skew of 950ps with a jitter of 380ps. At the system level with two White Sail boards communicating to each other, the worst-case condition between two slave DSL channels is a clock skew of 1.7ns with a peak to peak jitter of 720ps.

5 Test and Debug

5.1.1 Board Assembly

There will not be an in-circuit test (ICT) fixture designed for this board due to the limited quantity that will be assembled over the life of this product. As a result and in the interest of schedule only minimal effort will be spent on adding circuit-side test points to support such a fixture. Consequently, this will also limit the ability to perform tests on a flying-probe machine. Therefore, the assembly house will employ a 5DX x-ray machine to validate component placement and the quality of the soldering process. Normally, component values and type can be validated using a flying-probe machine (FPM). In lieu of the FPM, both the engineer and the assembly house will perform a visual inspection to validate the assembly of the board. It was deemed more critical to validate the quality of the solder joints with 5DX rather than component values with FPM, especially because the BGA cannot be inspected with the naked eye. This is made possible due to the nature of the design, i.e. there are a relatively small number of unique parts and the fact that there are eight typical circuits.

5.1.2 Board level features

5.1.2.1 Debug Mictor™ 1

The Mictor™ (38-pin connector) provides the user with visibility on specific signals using a logic analyzer. This particular Mictor™ allows the user to capture waveforms for: DEBUG [24:0] and the serial interface specified in the Silicon Laboratories' data sheet. In addition to the aforementioned signals, the serial enable signals for the master channel (channel 1) and Wave are available. The DEBUG bus is a general-purpose bus that runs between Wave and the FPGA in the system.

5.1.2.2 Debug Mictor™ 2

The Mictor™ (38-pin connector) provides the user with visibility on specific signals using a logic analyzer. This particular Mictor™ allows the user to capture waveforms

for: the nibble interface between Wave and the master DSL channel as well as the corresponding nibble interface between Wave and the FPGA in the main system. It also includes the reset signal for channel 1.

5.1.2.3 Test points

There are various test points to access the power rails and ground. These test points are strategically placed on the board and are labeled appropriately. There are no other test points in the design due to the compactness of the physical design.

5.1.2.4 Bring-up Checklist

The reader is deferred to the test plan and bring-up plan documents.

APPENDIX A: Bill of Materials

Item	QTY	Reference	Part	Manufacturer	Part Number	Stuff?
1	118	C1,C2,C3,C4,C21,C22,C23, C24,C25,C26,C27,C29,C37, C38,C48,C506,C515,C516, C517,C518,C519,C524,C526, C534,C535,C536,C537,C538, C539,C540,C543,C545,C553, C554,C555,C556,C557,C558, C559,C565,C566,C573,C574, C575,C576,C577,C578,C580, C584,C588,C587,C589,C590, C591,C593,C594,C596,C597, C598,C599,C602,C603,C605, C608,C607,C609,C610,C611, C612,C615,C616,C619,C620, C621,C623,C625,C626,C627, C629,C630,C631,C633,C634, C635,C644,C645,C648,C647, C648,C649,C652,C654,C662, C663,C664,C665,C666,C667, C668,C672,C674,C682,C683, C684,C685,C686,C687,C689, C694,C696,C697,C702,C703, C704,C705,C706,C707,C708	0.1uF	Venkel	C0805X7R250-104KNE	
2	16	C5,C8,C9,C10,C14,C15,C19, C20,C36,C41,C42,C43,C46, C47,C51,C52	2.2nF	Venkel	C0805C0G250-222JNE	
3	16	C7,C12,C17,C34,C39,C44, C49,C501,C504,C525,C544, C567,C636,C653,C673,C695	100u	AVX	TPSC107M010R0200	
4	15	C8,C13,C18,C35,C40,C45, C50,C505,C514,C521,C583, C595,C608,C613,C614	10uF	Venkel	C1210X7R160-106KNE	
5	3	C11,C16,C28	680u	Panasonic	EEV-FK1C681P	
6	2	C30,C32	33u	AVX	TPSB336K006R0600	
7	18	C31,C33,C520,C541,C560, C579,C585,C588,C592,C600, C601,C604,C622,C628,C655, C669,C688,C709	1u	TAIYO YUDEN	LMK212BJ105MG	
8	2	C502,C503	8.2pF	AVX	08055A8R2JAT2A	
9	16	C507,C508,C527,C528,C546, C547,C561,C569,C637,C638, C656,C657,C675,C676,C690, C698	18nF	Venkel	C1812C0G500-183JNE	
10	16	C509,C522,C523,C529,C542, C548,C562,C570,C639,C650, C651,C670,C671,C677,C691, C699	3.9nF	Venkel	C0805C0G250-392JNE	
11	17	C510,C513,C532,C533,C551, C552,C564,C571,C618,C640, C643,C659,C660,C678,C681, C693,C701	470pF	Venkel	C0805C0G500-471JNE	
12	16	C511,C512,C530,C531,C549, C550,C563,C572,C641,C642, C658,C661,C679,C680,C692, C700	3.3nF	Venkel	C0805C0G250-332JNE	
13	5	C568,C581,C582,C624,C632	0.01uF	Venkel	C0805X7R250-103KNE	
14	1	C617	47pF	AVX	08055A470JAT2A	
15	1	D1	GREEN	Dialight	550-0205	
16	3	D2,D3,D4	GREEN	Dialight	597-3301-102	
17	1	D5	RED	Dialight	597-3001-102	
18	2	D501,D502	Zener	Philips Semiconductor	BZX84-C6V2	
19	8	J1,J3,J4,J5,J11,J12,J13, J14	RJ45LED2	Tyco-AMP	405549-1	
20	1	J2	CPCI_RJ5			
21	1	J2	CPCI_RJ5	Tyco-AMP	646489-1	
22	1	J6	CON4	Tyco-AMP	770968-2	
23	2	J8,J7	2-767004-2	TYCO-AMP	2-767004-2	
24	1	J9	2-767004-5	Tyco-AMP	2-767004-5	
25	1	J10	Header6	Tyco-AMP	103148-6	
26	1	L1	1.2u	COILCRAFT	D01606T-102	
27	2	M501,M502	MMDF3N02HD	On Semiconductor	mmdf3n02hdr2	
28	16	R1,R2,R16,R17,R31,R32, R45,R46,R70,R71,R85,R86, R100,R101,R120,R121	27.4	Venkel	CR0805-8W-27R4FT	
29	16	R3,R4,R18,R19,R33,R34, R47,R48,R72,R73,R87,R88, R102,R103,R122,R123	0	Venkel	CR1210-2W-000FT	
30	16	R5,R8,R22,R23,R37,R38, R50,R51,R74,R77,R90,R91, R104,R107,R126,R127	60.4	Venkel	CR0805-8W-60R4FT	
31	16	R6,R7,R20,R21,R35,R36, R49,R52,R75,R76,R89,R92, R105,R106,R124,R125	1	Venkel	CR0805-8W-1R0FT	

32	79	R9,R10,R24,R25,R39,R40, R53,R54,R60,R64,R66,R78, R79,R93,R94,R108,R109, R114,R115,R116,R117,R118, R128,R129,R134,R135,R136, R137,R138,R509,R512,R521, R523,R526,R530,R534,R536, R539,R545,R548,R551,R555, R558,R559,R571,R576,R579, R582,R595,R604,R606,R608, R610,R611,R617,R619,R623, R624,R625,R626,R627,R628, R629,R630,R631,R635,R636, R637,R638,R639,R640,R642, R643,R644,R645,R646,R647, R650,R658	200	Venkel	CR0805-8W-2000FT	
33	16	R11,R12,R26,R27,R41,R42, R55,R56,R80,R81,R95,R96, R110,R111,R130,R131	2 43	Venkel	CR1206-4W-2R43FT	
34	16	R13,R14,R28,R29,R43,R44, R57,R58,R82,R97,R98,R99, R112,R113,R132,R133	49 9	Venkel	CR0805-8W-49R9FT	
35	29	R15,R61,R85,R119,R517, R518,R520,R527,R556,R557, R560,R574,R578,R580,R585, R586,R587,R607,R616,R653, R654,R655,R656,R657,R667, R668,R669,R670,R671	1 15k	Venkel	CR0805-8W-1151FT	
36	6	R30,R511,R515,R516,R525, R602	200	Venkel	CR0805-8W-2000FT	NO_LOAD
37	31	R59,R62,R83,R552,R553, R554,R561,R562,R563,R564, R565,R566,R567,R568,R569, R570,R572,R573,R575,R577, R581,R583,R584,R597,R598, R599,R600,R612,R613,R614, R615	43	Venkel	CR0805-8W-43R0FT	
38	3	R67,R593,R601	4 02k	Venkel	CR0805-8W-4021FT	
39	1	R68	7 68k	Venkel	CR0805-8W-7681FT	
40	1	R69	100k	Venkel	CR0805-8W-1003FT	
41	2	R83,R594	73 2k	Venkel	CR0805-8W-7322FT	
42	1	R84	1 43k	Venkel	CR0805-8W-1431FT	
43	16	R501,R502,R503,R504,R505, R506,R507,R508,R659,R660, R661,R662,R663,R664,R665, R666	10M	Venkel	CR0805-8W-106JT	
44	16	R510,R513,R514,R522,R524, R531,R540,R546,R618,R620, R621,R632,R633,R641,R648, R651	4 99k	Venkel	CR0805-8W-4991FT	
45	8	R519,R529,R532,R547,R622, R634,R649,R652	21k	Venkel	CR0805-8W-2102FT	
46	1	R528	1 15k	Venkel	CR0805-8W-1151FT	NO_LOAD
47	3	R533,R535,R596	2 21k	Venkel	CR0805-8W-2211FT	
48	2	R537,R538	10	Venkel	CR0805-8W-10R0FT	
49	3	R541,R543,R544	1k	Venkel	CR0805-8W-1001FT	
50	2	R542,R550	0 028	Vishay-Dale	WSL1206R028	
51	1	R549	10k	Venkel	CR0805-8W-1002FT	
52	1	R588	0	Venkel	CR0805-8W-000FT	
53	1	R589	15k	Venkel	CR0805-8W-1502FT	
54	2	R590,R592	174k	Venkel	CR0805-8W-1743FT	
55	1	R591	200k	Venkel	CR0805-8W-2003FT	
56	1	R603	39 2k	Venkel	CR0805-8W-3922FT	
57	2	R609,R605	26 1k	Venkel	CR0805-8W-2612FT	
58	2	SW2,SW1	SPST_MOM	ITT Cannon	KT11B1SAM	
59	2	SW4,SW3	DIP_SW8	ITT Industries, Cannon	tda08h0sk1	
60	11	TP1,TP2,TP3,TP4,TP5,TP6, TP7,TP8,TP9,TP10,TP11	TestPoint			NO_LOAD
61	8	T1,T2,T3,T4,T5,T6,T7,T8	Midcom_51572	Midcom	51572 rev2	
62	8	U1,U2,U3,U4,U15,U17,U18, U21	Si3101_RevE	Silicon Laboratories	si3101-KQ	
63	2	U5,U6	CY2304-1	Cypress	CY2304SC-1	
64	1	U7	74LVT244A/TSO	Fairchild Semiconductor	74LVTH244MTC	
65	1	U8	TinyAND3	Fairchild Semiconductor	NC7SZ11P8X	
66	1	U9	XC2V1000			
67	1	U9	XC2V1000	Xilinx	XC2V1000-5BG575C	
68	2	U20,U10	LVC1G04	Texas Instruments	SN74LVC1G04DBVR	
69	1	U11	CY7B991V	Cypress	cy7b991v-2jc	
70	3	U12,U13,U16	MIC2778_1BM5	Micrel	MIC2778-1BM5	
71	1	U14	LTC3411	Linear Technology	LTC3411EMS	
72	2	U19,U504	QS3VH861	IDT	IDTQS3VH861Q	
73	1	U501	LTC1646	Linear Technology	ltc1646cgn	
74	1	U502	MPC947	Motorola	mpc947fa	
75	1	U503	XC18V04VQ44C	Xilinx	XC18V04VQ44C	
76	1	Y1	Crystal	ECS	ECS-088 32-CD-0277	

APPENDIX B: Component to Schematics Cross Reference

Ref Des	Part	Page	Ref Des	Part	Page	Ref Des	Part	Page	Ref Des	Part	Page	Ref Des	Part	Page	Ref Des	Part	Page
C1	0 1uF	4	C559	0 1uF	8	C629	1u	10	R46	27 4	7	R518	1 15k	4	R828	200	3
C2	0 1uF	2	C560	1u	8	C670	3 9nF	9	R47	0	7	R519	21k	4	R829	200	3
C3	0 1uF	2	C561	18nF	7	C671	3 9nF	10	R48	0	7	R520	1 15k	4	R830	200	10
C4	0 1uF	2	C562	3 9nF	7	C672	0 1uF	10	R49	1	7	R521	200	5	R831	200	9
C5	2 2nF	4	C563	3 3nF	7	C673	100u	10	R50	60 4	7	R522	4 99k	5	R832	4 99k	9
C6	2 2nF	4	C564	470pF	7	C674	0 1uF	9	R51	60 4	7	R523	200	5	R833	4 99k	10
C7	100u	10	C565	0 1uF	7	C675	18nF	10	R52	1	7	R524	4 99k	6	R834	21k	9
C8	10uF	5	C566	0 1uF	7	C676	18nF	10	R53	200	7	R525	200	5	R835	200	3
C9	2 2nF	5	C567	100u	7	C677	3 9nF	10	R54	200	7	R526	200	5	R836	200	3
C10	2 2nF	5	C568	0 01uF	15	C678	470pF	10	R55	2 43	7	R527	1 15k	5	R837	200	3
C11	680u	15	C569	18nF	7	C679	3 3nF	10	R56	2 43	7	R528	1 15k	5	R838	200	3
C12	100u	9	C570	3 9nF	7	C680	3 3nF	10	R57	49 9	7	R529	21k	5	R839	200	3
C13	10uF	8	C571	470pF	7	C681	470pF	10	R58	49 9	7	R530	200	6	R840	200	3
C14	2 2nF	6	C572	3 3nF	7	C682	0 1uF	10	R59	43	3	R531	4 99k	6	R841	4 99k	10
C15	2 2nF	6	C573	0 1uF	7	C683	0 1uF	10	R60	200	3	R532	21k	6	R842	200	3
C16	680u	15	C574	0 1uF	7	C684	0 1uF	10	R61	1 15k	3	R533	2 21k	15	R843	200	3
C17	100u	8	C575	0 1uF	7	C685	0 1uF	10	R62	43	3	R534	200	15	R844	200	3
C18	10uF	7	C576	0 1uF	7	C686	0 1uF	10	R63	43	3	R535	2 21k	15	R845	200	3
C19	2 2nF	7	C577	0 1uF	7	C687	0 1uF	10	R64	200	13	R536	200	15	R846	200	11
C20	2 2nF	7	C578	0 1uF	7	C688	1u	8	R65	1 15k	14	R537	10	15	R847	200	10
C21	0 1uF	3	C579	1u	7	C689	0 1uF	15	R66	200	13	R538	10	15	R848	4 99k	11
C22	0 1uF	3	C580	0 1uF	15	C690	18nF	11	R67	4 02k	13	R539	200	8	R849	21k	10
C23	0 1uF	3	C581	0 01uF	15	C691	3 9nF	11	R68	7 68k	15	R540	4 99k	7	R850	200	11
C24	0 1uF	3	C582	0 01uF	15	C692	3 3nF	11	R69	100k	15	R541	1k	15	R851	4 99k	11
C25	0 1uF	3	C583	10uF	12	C693	470pF	11	R70	27 4	8	R542	0 028	15	R852	21k	11
C26	0 1uF	3	C584	0 1uF	12	C694	0 1uF	11	R71	27 4	8	R543	1k	15	R853	1 15k	15
C27	0 1uF	3	C585	1u	12	C695	100u	11	R72	0	8	R544	1k	15	R854	1 15k	15
C28	680u	15	C586	0 1uF	12	C696	0 1uF	10	R73	0	8	R545	200	7	R855	1 15k	15
C29	0 1uF	15	C587	0 1uF	12	C697	0 1uF	15	R74	60 4	8	R546	4 99k	7	R856	1 15k	15
C30	33u	15	C588	1u	12	C698	18nF	11	R75	1	8	R547	21k	7	R857	1 15k	15
C31	1u	15	C589	0 1uF	12	C699	3 9nF	11	R76	1	8	R548	200	15	R858	200	15
C32	33u	15	C590	0 1uF	12	C700	3 3nF	11	R77	60 4	8	R549	10k	15	R859	10M	2
C33	1u	15	C591	0 1uF	12	C701	470pF	11	R78	200	8	R550	0 028	15	R860	10M	2
C34	100u	5	C592	1u	12	C702	0 1uF	11	R79	200	8	R551	200	7	R861	10M	2
C35	10uF	8	C593	0 1uF	12	C703	0 1uF	11	R80	2 43	8	R552	43	3	R862	10M	2
C36	2 2nF	8	C594	0 1uF	12	C704	0 1uF	11	R81	2 43	8	R553	43	3	R863	10M	2
C37	0 1uF	15	C595	10uF	12	C705	0 1uF	11	R82	49 9	8	R554	43	3	R864	10M	2
C38	0 1uF	15	C596	0 1uF	3	C706	0 1uF	11	R83	73 2k	15	R555	200	13	R865	10M	2
C39	100u	7	C597	0 1uF	12	C707	0 1uF	11	R84	1 43k	15	R556	1 15k	13	R866	10M	2
C40	10uF	9	C598	0 1uF	12	C708	0 1uF	11	R85	27 4	9	R557	1 15k	13	R867	1 15k	15
C41	2 2nF	8	C599	0 1uF	12	C709	1u	11	R86	27 4	9	R558	200	13	R868	1 15k	15
C42	2 2nF	9	C600	1u	12	D1	GREEN	15	R87	0	9	R559	200	3	R869	1 15k	15
C43	2 2nF	9	C601	1u	12	D2	GREEN	15	R88	0	9	R560	1 15k	3	R870	1 15k	15
C44	100u	8	C602	0 1uF	12	D3	GREEN	15	R89	1	9	R561	43	3	R871	1 15k	15
C45	10uF	10	C603	0 1uF	12	D4	GREEN	13	R90	60 4	9	R562	43	3	SW1	SPST_MOM	15
C46	2 2nF	10	C604	1u	12	D5	RED	15	R91	60 4	9	R563	43	3	SW2	SPST_MOM	15
C47	2 2nF	10	C605	0 1uF	14	D501	Zener	15	R92	1	9	R564	43	3	SW3	DIP_SW8	3
C48	0 1uF	15	C606	0 1uF	14	D502	Zener	15	R93	200	9	R565	43	3	SW4	DIP_SW8	3
C49	100u	4	C607	0 1uF	3	J1	RJ45LED2	4	R94	200	9	R566	43	3	TP1	TestPoint	14
C50	10uF	11	C608	10uF	12	J2	CPCI_RJ5	2	R95	2 43	9	R567	43	3	TP2	TestPoint	14
C51	2 2nF	11	C609	0 1uF	12	J3	RJ45LED2	5	R96	2 43	9	R568	43	3	TP3	TestPoint	14
C52	2 2nF	11	C610	0 1uF	12	J4	RJ45LED2	6	R97	49 9	8	R569	43	3	TP4	TestPoint	14
C501	100u	4	C611	0 1uF	12	J5	RJ45LED2	7	R98	49 9	9	R570	43	3	TP5	TestPoint	14
C502	8 2pF	4	C612	0 1uF	12	J6	CON4	15	R99	49 9	9	R571	200	14	TP6	TestPoint	14
C503	8 2pF	4	C613	10uF	12	J7	2-767004-2	13	R100	27 4	10	R572	43	14	TP7	TestPoint	14
C504	100u	11	C614	10uF	3	J8	2-767004 2	13	R101	27 4	10	R573	43	3	TP8	TestPoint	14
C505	10uF	2	C615	0 1uF	13	J9	2-767004-5	14	R102	0	10	R574	1 15k	14	TP9	TestPoint	14
C506	0 1uF	2	C616	0 1uF	13	J10	Header6	13	R103	0	10	R575	43	14	TP10	TestPoint	14
C507	10nF	4	C617	47pF	15	J11	RJ45LED2	8	R104	60 4	10	R576	200	14	TP11	TestPoint	14
C508	18nF	4	C618	470pF	15	J12	RJ45LED2	9	R105	1	10	R577	43	3	T1	Midcom_51572	4
C509	3 9nF	4	C619	0 1uF	15	J13	RJ45LED2	10	R106	1	10	R578	1 15k	14	T2	Midcom_51572	5
C510	470pF	4	C620	0 1uF	12	J14	RJ45LED2	11	R107	60 4	10	R579	200	13	T3	Midcom_51572	6
C511	3 3nF	4	C621	0 1uF	3	L1	1 2u	15	R108	200	10	R580	1 15k	13	T4	Midcom_51572	7
C512	3 3nF	4	C622	1u	12	M501	MMDF3N02HD	15	R109	200	10	R581	43	14	T5	Midcom_51572	8
C513	470pF	4	C623	0 1uF	12	M502	MMDF3N02HD	15	R110	2 43	10	R582	200	13	T6	Midcom_51572	9
C514	10uF	4	C624	0 01uF	3	R1	27 4	4	R111	2 43	10	R583	43	14	T7	Midcom_51572	10
C515	0 1uF	4	C625	0 1uF	12	R2	27 4	4	R112	49 9	10	R584	43	14	T8	Midcom_51572	11
C516	0 1uF	4	C626	0 1uF	3	R3	0	4	R113	49 9	10	R585	1 15k	13	U1	Si3101_RevE	4
C517	0 1uF	4	C627	0 1uF	3	R4	0	4	R114	200	15	R586	1 15k	13	U2	Si3101_RevE	5
C518	0 1uF	4	C628	1u	12	R5	60 4	4	R115	200	15	R587	1 15k	13	U3	Si3101_RevE	6
C519	0 1uF	4	C629	0 1uF	3	R6	1	4	R116	200	15	R588	0	15	U4	Si3101_RevE	7
C520	1u	4	C630	0 1uF	13	R7	1	4	R117	200	15	R589	15k	15	U5	CY2304 1	3

C522	3 9nF	4	C632	0 01uF	3	R9	200	4	R119	1 15k	15	R591	200k	15	U7	74LVT244ATSO	14
C523	3 9nF	5	C633	0 1uF	3	R10	200	4	R120	27 4	11	R592	174k	15	U8	TinyAND3	14
C524	0 1uF	4	C634	0 1uF	3	R11	2 43	4	R121	27 4	11	R593	4 02k	15	U9	XC2V1000	12,13
C525	100u	5	C635	0 1uF	13	R12	2 43	4	R122	0	11	R594	73 2k	15	U10	LVC1G04	13
C526	0 1uF	4	C636	100u	8	R13	49 9	4	R123	0	11	R595	200	15	U11	CY7B991V	3
C527	18nF	5	C637	18nF	8	R14	49 9	4	R124	1	11	R596	2 21k	15	U12	MIC2778_1BM5	15
C528	18nF	5	C638	18nF	8	R15	1 15k	5	R125	1	11	R597	43	3	U13	MIC2778_1BM5	15
C529	3 9nF	5	C639	3 9nF	8	R16	27 4	5	R126	60 4	11	R598	43	3	U14	LTC3411	15
C530	3 3nF	5	C640	470pF	8	R17	27 4	5	R127	60 4	11	R599	43	3	U15	Si3101_RevE	6
C531	3 3nF	5	C641	3 3nF	8	R18	0	5	R128	200	11	R600	43	3	U16	MIC2778_1BM5	15
C532	470pF	5	C642	3 3nF	8	R19	0	5	R129	200	11	R601	4 02k	13	U17	Si3101_RevE	9
C533	470pF	5	C643	470pF	8	R20	1	5	R130	2 43	11	R602	200	15	U18	Si3101_RevE	10
C534	0 1uF	5	C644	0 1uF	8	R21	1	5	R131	2 43	11	R603	39 2k	15	U19	QS3VH861	15
C535	0 1uF	5	C645	0 1uF	8	R22	60 4	5	R132	49 9	11	R604	200	15	U20	LVC1G04	15
C536	0 1uF	5	C646	0 1uF	8	R23	60 4	5	R133	49 9	11	R605	26 1k	15	U21	Si3101_RevE	11
C537	0 1uF	5	C647	0 1uF	8	R24	200	5	R134	200	15	R606	200	15	U501	LTC1646	15
C538	0 1uF	5	C648	0 1uF	8	R25	200	5	R135	200	15	R607	1 15k	15	U502	MPC947	3
C539	0 1uF	5	C649	0 1uF	8	R26	2 43	5	R136	200	15	R608	200	15	U503	XC18V04VO44C	13
C540	0 1uF	5	C650	3 9nF	8	R27	2 43	5	R137	200	15	R609	26 1k	15	U504	QS3VH861	15
C541	1u	5	C651	3 9nF	9	R28	49 9	5	R138	200	15	R610	200	15	Y1	Crystal	4
C542	3 9nF	6	C652	0 1uF	8	R29	49 9	5	R501	10M	2	R611	200	3			
C543	0 1uF	6	C653	100u	9	R30	200	5	R502	10M	2	R612	43	3			
C544	100u	6	C654	0 1uF	8	R31	27 4	6	R503	10M	2	R613	43	3			
C545	0 1uF	5	C655	1u	9	R32	27 4	6	R504	10M	2	R614	43	3			
C546	18nF	6	C656	18nF	9	R33	0	6	R505	10M	2	R615	43	3			
C547	18nF	6	C657	18nF	9	R34	0	6	R506	10M	2	R616	1 15k	13			
C548	3 9nF	6	C658	3 3nF	9	R35	1	6	R507	10M	2	R617	200	8			
C549	3 3nF	6	C659	470pF	9	R36	1	6	R508	10M	2	R618	4 99k	8			
C550	3 3nF	6	C660	470pF	9	R37	60 4	6	R509	200	4	R619	200	8			
C551	470pF	6	C661	3 3nF	9	R38	60 4	6	R510	4 99k	4	R620	4 99k	8			
C552	470pF	6	C662	0 1uF	9	R39	200	6	R511	200	4	R621	4 99k	9			
C553	0 1uF	6	C663	0 1uF	9	R40	200	6	R512	200	4	R622	21k	8			
C554	0 1uF	6	C664	0 1uF	9	R41	2 43	6	R513	4 99k	4	R623	200	3			
C555	0 1uF	6	C665	0 1uF	9	R42	2 43	6	R514	4 99k	5	R624	200	3			
C556	0 1uF	6	C666	0 1uF	9	R43	49 9	6	R515	200	4	R625	200	9			
C557	0 1uF	6	C667	0 1uF	9	R44	49 9	6	R516	200	4	R626	200	3			
C558	0 1uF	6	C668	0 1uF	9	R45	27 4	7	R517	1 15k	4	R627	200	3			

WhiteSail
Layout Guidelines

WhiteSail Card Layout Guidelines

Table of Contents

1 Introduction

This document presents guidelines for use during the layout phase of the WhiteSail board lifecycle. The layout guidelines should be applied in conjunction with any notes or remarks that may be found in the corresponding schematics. Any information in this document that is inconsistent with the notes in the schematics should be brought to the attention of the designer. However, the schematics shall override the instructions in this document.

2 Board Construction

2.1 Mechanical Specifications

This board is a standard Compact PCI, 6U, rear I/O card. Therefore, the board's form factor shall conform to the Compact PCI specification 2.0, which also refers to IEEE specifications 1101.10 and 1101.11.

2.2 Stack Up

The fabrication vendor according to the following specifications shall design the board's layer construction:

- Target impedance = 50 Ohms +/- 10%
- Board thickness = 1.6mm +/- 0.2 mm
- Layer count = 12

2.3 Plane Cutouts and Shapes

The following diagram/table highlights the plane cutouts
GND
VD1P5
VD3P3
VD3P3_BP
VA5P0
VA5P0_BP
ESD_STRIP_L1
ESD_STRIP_L2
ESD_STRIP_L3
ESD_STRIP_R1
ESD_STRIP_R2
ESD_STRIP_R3

2.4 Additional Ground Shielding

The surfaces should be filled with ground shapes primarily to isolate the channels from each other. Also, all clock buffers and Silicon Laboratories devices should have a ground shape directly beneath the physical package. These buffers include: CY2304, CY7B991, and MPC947.

3 Placement

3.1 Test Points

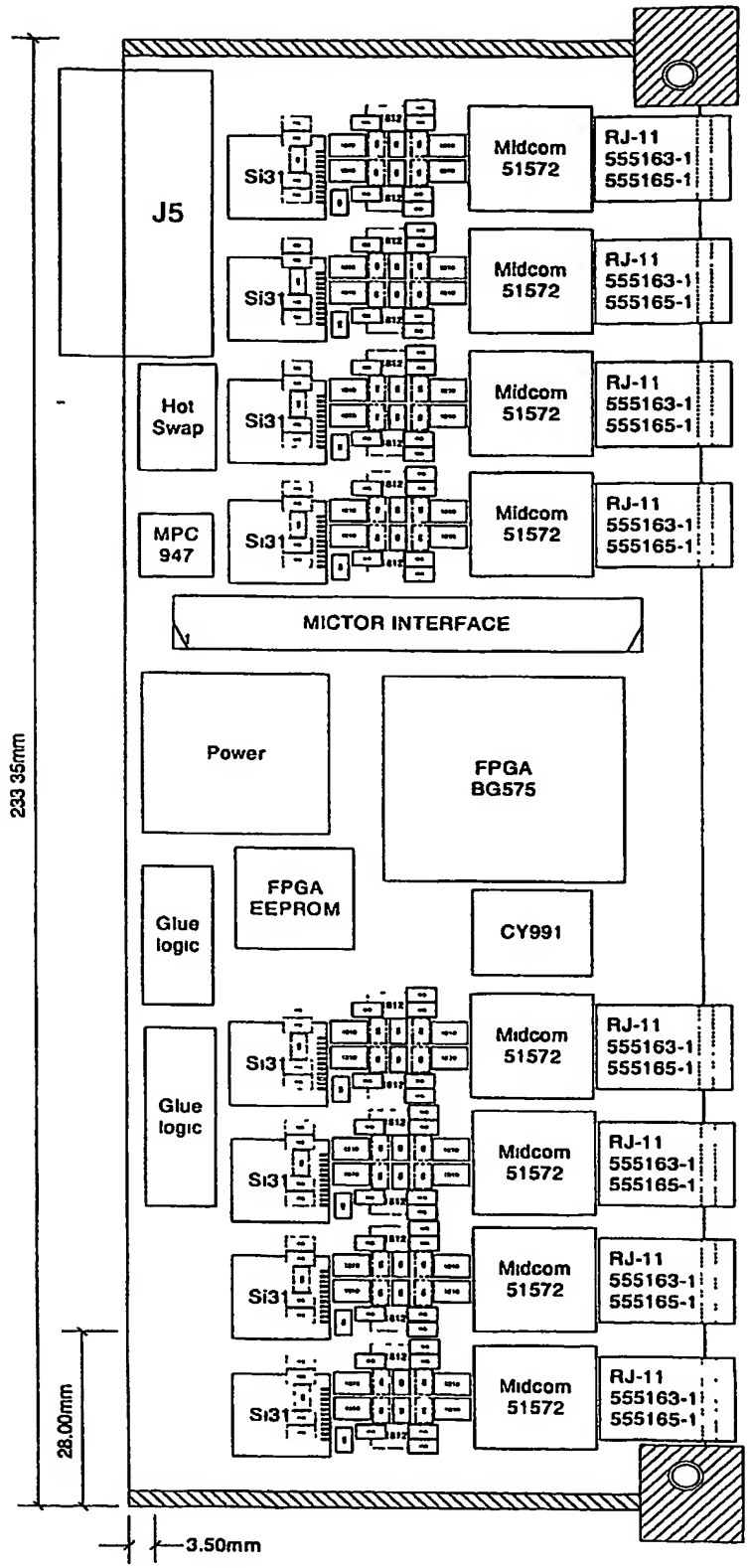
There shall be several test points strategically placed on the board. Refer to the following table for the placement of certain test points. Note that the X-Y coordinates that are listed serve as a marker. Due to the presence of signals and devices the actual placement of the test point can deviate from the marker by 0.5".

Test Point	X-Coor	Y-Coor	Label
TP11	1.0"	0.0"	GND
TP10	1.0"	2.0"	GND
TP9	2.0"	2.0"	GND
TP4	1.0"	4.0"	GND
TP5	2.0"	4.0"	GND
TP1	1.0"	6.0"	GND
TP7	1.0"	3.0"	3.3V
TP2	1.0"	6.0"	3.3V
TP8	1.25"	3.0"	5.0V
TP3	1.25"	6.0"	5.0V
TP6	Flexible	Flexible	1.5V

3.2 Placement Diagram

The following figure shows how the majority of the components or blocks of circuits should be placed. This is a general guideline thus the layout designer has the liberty of optimizing placement for ease of routing. There are eight typical circuits in the design which implies that the layout should only be done for one circuit and then replicated to produce the remaining circuits. This suggests that placement should be duplicated exactly as in the first circuit such that routing can then be replicated as well.

WhiteSail Card Layout Guidelines



3.3 Analog Circuit

There are a total of eight channels in the design each of which uses the analog circuit shown below. This circuit requires particular attention during layout as described below.

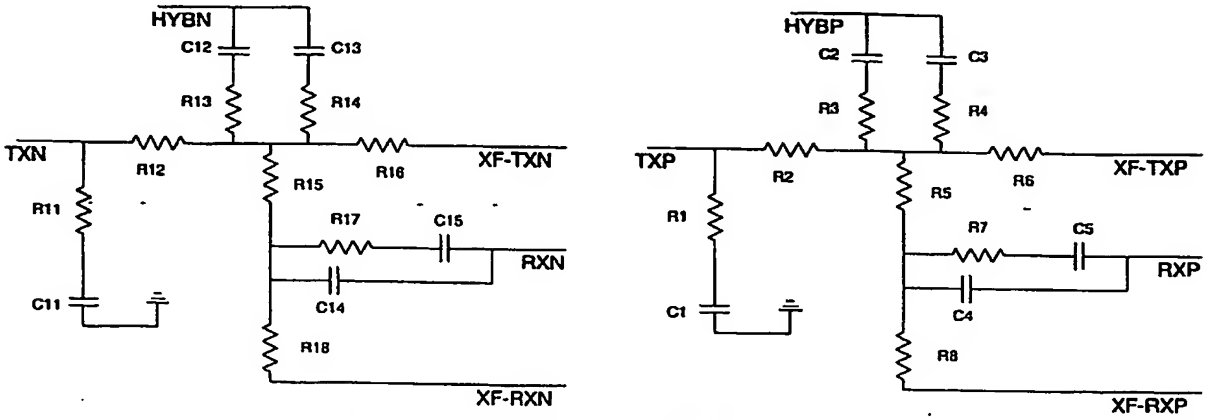


Figure 1: Typical Analog Circuit

The following diagram shows some suggested ways of placing the components that make up the analog circuit. The characteristics of the layout consist of the following:

- Exact symmetry during placement
- As compact as possible without compromising manufacturability
- Share surface shapes to minimize the number of vias used
- Matched traces at the different circuit nodes
- Ground flooding around the circuit

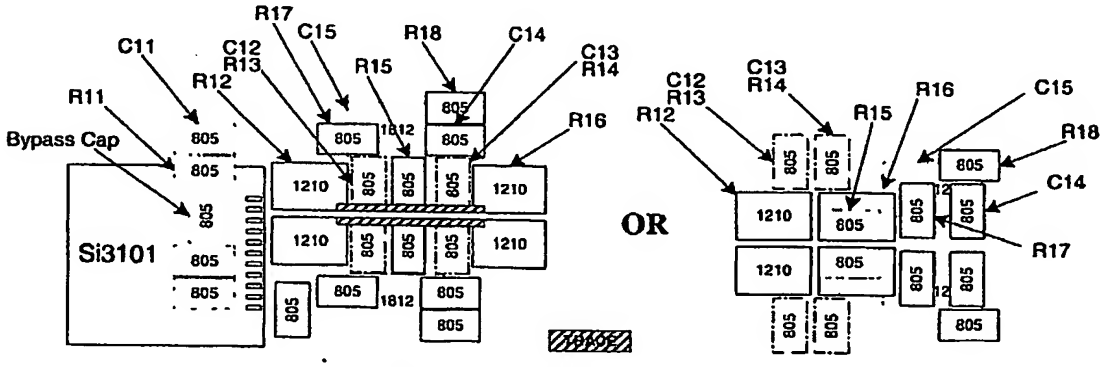


Figure 2: Placement Examples

The transformer and user interface lies on the other end of the analog circuit. All voltage planes and ground planes should be cut away from beneath these two components except near the analog to transformer interface. These cutouts should be 50 mils larger than the external dimensions of the components.

3.4 Power and Hot Swap

Both the power regulator and the hot swap controller should be implemented as described in the respective data sheets. In addition to these instructions, the following guidelines should be referenced for the power regulator.

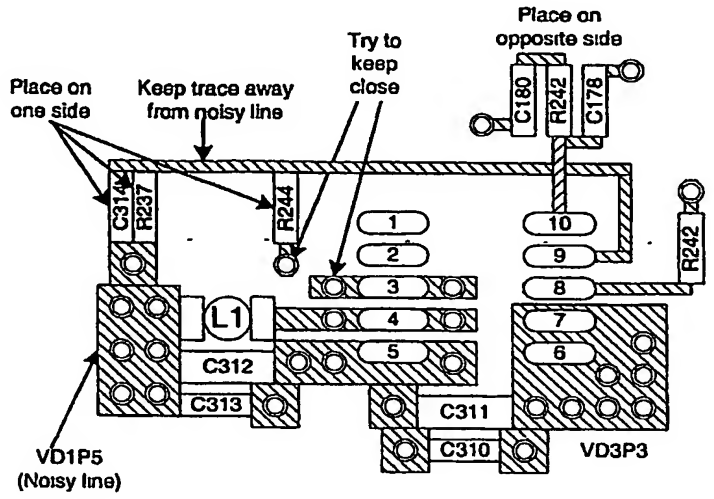


Figure 3

The shapes or etchings shown in the figure above are for reference only and can be formed in any compact manner to accommodate the via count. The actual layout may deviate slightly due to other components and traces that are not related to this circuitry. There will also be deviations due to the fact that this drawing is not to scale.

The traces off of pins 1, 2, 8, 9, 10 may be as wide or wider than the minimum trace width for the respective routing layer. The traces off of pins 3 and 4 should be routed as wide as physically possible from the device pad. Pins 5, 6, and 7 should use shapes in a similar manner as shown above. The passives connected to pin 10 should be placed as close as possible to the pad.

3.5 External Interfaces

3.5.1 Secondary Power Connecter

The 2x2 power connecter (AMP 770968-2) should be placed along the back plane interface without hanging over the edge of the board. This should also be located near the associated hot swap circuitry.

3.5.2 FPGA Programming Header

The 1x6 header (AMP 103148-6) should be placed along the front of the card without hanging over the edge of the board.

3.5.3 DSL channel interfaces

Each DSL channel interface consists of an RJ45 connector with integrated LED devices. The RJ45 shall hang over the edge of the board so that it protrudes through the faceplate.

4 Signal Guidelines

4.1 Clocks and Resets

The proceeding groups of signals shall have the following characteristics:
Impedance: 50 Ohms
Matching Tolerance: +/- 100 mil
Routing Layer: Inner layer stripe-line
Trace separation: 15 mil spacing

4.1.1 Group1: Match to 5.5"

- ROBO_DSL*_MINCLK35M
- BUF4B_DMR*
- BUF4B_FG_DSL1_MCLK

4.1.2 Group 2: Match to 2.0"

- BUF4A_ROBO_MCLK35M
- DSL1_BUF4A_MR_MCLK
- BUF4A_BUF4B_MCLK

4.1.3 Group 3: Match to 6.0"

- BUF4A_FDBK_MCLK35M
- BUF4B_FDBK_MCLK35M
- ROBO_FDBK

4.1.4 Group 4: Match to longest trace in the group

Note: +/- 250 mil tolerance

- BUF_DSL*_SCLK
- BUF_FPGA_SCLK
- BUF_DMR2_SCLK

4.1.5 Group 5: Match to longest trace in the group

Note: +/- 400 mil tolerance

- BUF_EPRM_TCK
- BUF_FPGA_TCK

4.1.6 Group 6: Match to longest trace in the group

Note: +/- 200 mil tolerance; minimum spacing allowed

- QS_FG_*_RST_L

4.1.7 Group 7: Match to longest trace in the group

Note: +/- 200 mil tolerance; minimum spacing allowed

- MR_QS_*_RST_L

4.1.8 Group 8: Match to longest trace in the group

Note: +/- 200 mil tolerance; minimum spacing allowed

- FG_DSL*_RST_L

4.2 Single Nets

The proceeding signals shall have the following characteristics:
Impedance: 50 Ohms
Matching Tolerance: +/- 100 mil
Routing Layer: Inner layer stripe-line
Trace separation: 15 mil spacing

4.2.1 Signal 1: Length of 4.5"

- DSL1_SI_BUF_MCLK

4.3 Data busses

The proceeding groups of signals shall have the following characteristics:
Impedance: 50 Ohms
Matching Tolerance: +/- 100 mil
Routing Layer: Inner layer stripe-line
Trace separation: 15 mil spacing preferred, 10 mil spacing allowed

4.3.1 Group 1: Match to longest trace in the group

Note: +/- 200 mil matching tolerance

- DSL1_SI_FG_*
- DSL1_FG_SI_*

4.3.2 Group 2: Match to longest trace in the group

Note: +/- 200 mil matching tolerance

- DSL2_SI_FG_*
- DSL2_FG_SI_*

4.3.3 Group 3: Match to longest trace in the group

Note: +/- 200 mil matching tolerance

- DSL3_SI_FG_*
- DSL3_FG_SI_*

4.3.4 Group 4: Match to longest trace in the group

Note: +/- 200 mil matching tolerance

- DSL4_SI_FG_*
- DSL4_FG_SI_*

4.3.5 Group 5: Match to longest trace in the group

Note: +/- 200 mil matching tolerance

- DSL5_SI_FG_*
- DSL5_FG_SI_*

4.3.6 Group 6: Match to longest trace in the group

Note: +/- 200 mil matching tolerance

- DSL6_SI_FG_*

- DSL6_FG_SI_*

4.3.7 Group 7: Match to longest trace in the group

Note: +/- 200 mil matching tolerance

- DSL7_SI_FG_*
- DSL7_FG_SI_*

4.3.8 Group 8: Match to longest trace in the group

Note: +/- 200 mil matching tolerance

- DSL8_SI_FG_*
- DSL8_FG_SI_*

4.4 Analog Signals

4.4.1 Group 1: Match to longest trace in the group

Note: +/- 5 mil matching tolerance

- DSL8_ DEV_RX*

4.4.2 Group 2: Match to longest trace in the group

Note: +/- 5 mil matching tolerance

- DSL8_ DEV_HYB*

4.4.3 Group 3: Match to longest trace in the group

Note: +/- 5 mil matching tolerance

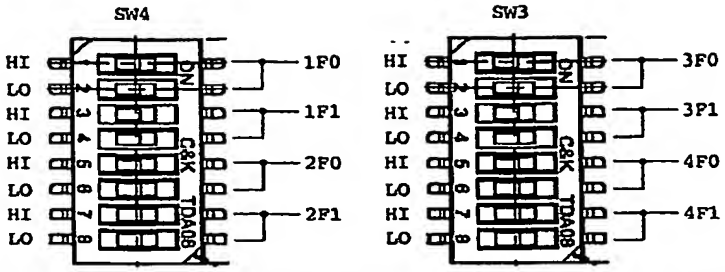
- DSL8_ DEV_TX*

4.4.4 Replicate groups 1 through 3

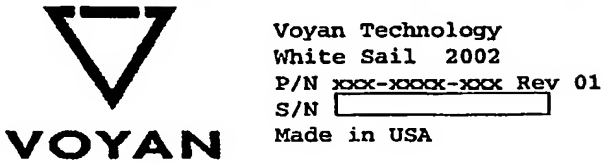
Each analog channel comprises of groups 1 through 3 above. Since there are eight channels total, the differential signals in the analog layout will be replicated seven more times.

5 Silkscreen

- All reference designators are to be renumbered in ascending order using the top, left-hand corner of the form factor as a reference point. Also, devices on the backside (circuit side) should start their numbering sequence at 500 (i.e. R500, C500, U500, etc).
- Polarized capacitors should include a marker to denote the polarity.
- Diodes and LED's should include a marker to denote cathode versus anode
- The DIP-switch settings should be included as shown in the proceeding figure. A representation of the device can be drawn elsewhere on the board if the text cannot be placed near the actual device.



- Assembly information should be included as shown in the proceeding figure.



- BGA numbering should also be shown on the bottom side of the board
- Labels should be added according to the following table:

Device	Label
J10-1	VDD
J10-2	TCK
J10-3	TMS
J10-4	TDI
J10-5	TDO
J10-6	GND
D4	DONE
D5	PWR_RST
D1	PWR_GOOD
D2	5.0V
D3	3.3V
SW1	PWR_CYCLE
SW2	RESET
J6-1	5.0V
J6-2	GND
J6-3	3.3V
J6-4	GND

- Each DSL channel should be labeled near the RJ45 connector using the text "DSLx", where x denotes the channel number
- Test points should also be labeled as discussed above. The table is repeated here for convenience.

Test Point	X-Coor	Y-Coor	Label
TP11	1.0"	0.0"	GND
TP10	1.0"	2.0"	GND
TP9	2.0"	2.0"	GND
TP4	1.0"	4.0"	GND
TP5	2.0"	4.0"	GND
TP1	1.0"	6.0"	GND
TP7	1.0"	3.0"	3.3V
TP2	1.0"	6.0"	3.3V

TP8	1.25"	3.0"	5.0V
TP3	1.25"	6.0"	5.0V
TP6	Flexible	Flexible	1.5V

WHITE SAIL SCHEMATICS

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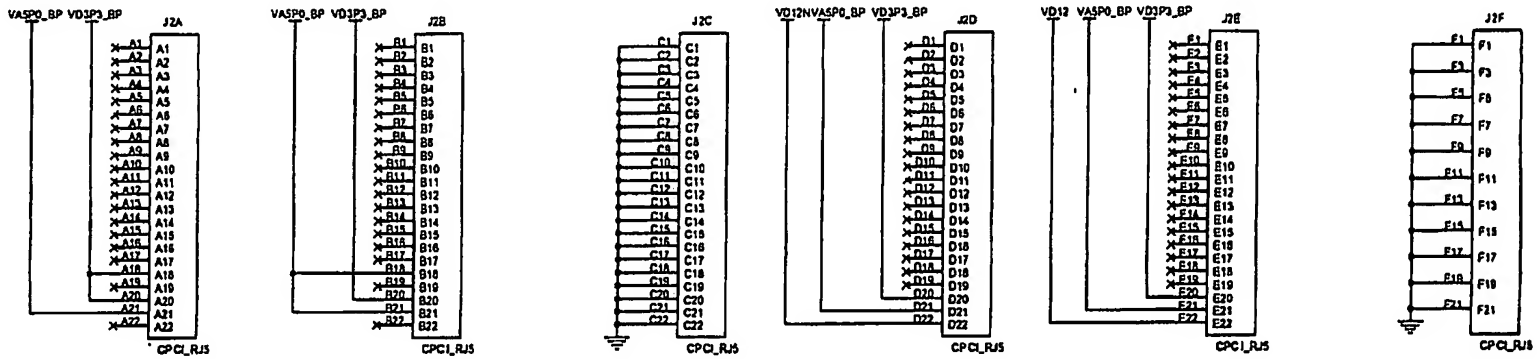

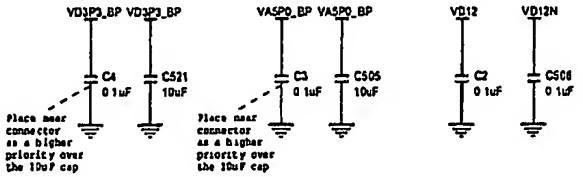

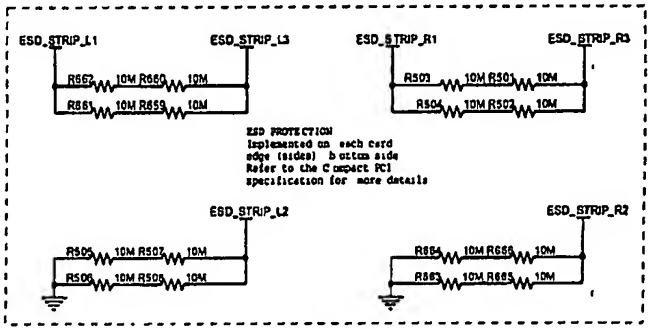

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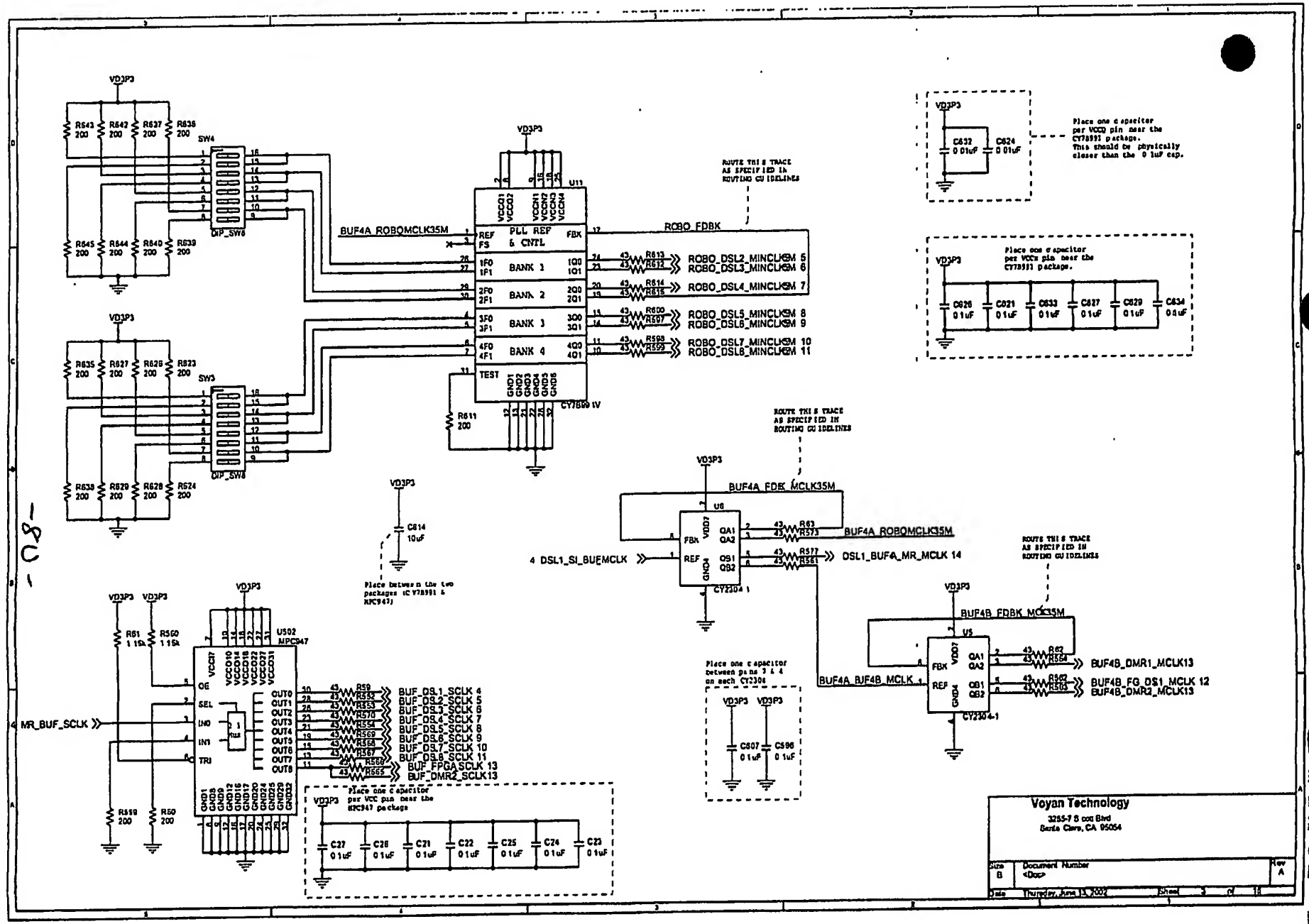
VD3P3
R643 200
R642 200
R637 200
R636 200
SW4
DIP_SW8
R645 200
R644 200
R640 200
R639 200
BUF4A_ROBOMCLK35M
U11
PLL REF & CNTL
REF
FS
FBK
ROBO_FDBK
1F0
1F1
BANK 1
1Q0
1Q1
ROBO_DSL2_MINCLKSM 5
ROBO_DSL3_MINCLKSM 6
2F0
2F1
BANK 2
2Q0
2Q1
ROBO_DSL4_MINCLKSM 7
3F0
3F1
BANK 3
3Q0
3Q1
ROBO_DSL5_MINCLKSM 8
ROBO_DSL6_MINCLKSM 9
4F0
4F1
BANK 4
4Q0
4Q1
ROBO_DSL7_MINCLKSM 10
ROBO_DSL8_MINCLKSM 11
TEST
CY7B991V
R611 200
ROUTE THIS TRACE AS SPECIFIED IN ROUTING GUIDELINES
R635 200
R627 200
R626 200
R623 200
SW3
DIP_SW8
R638 200
R629 200
R628 200
R624 200
C632 0.01uF
C624 0.01uF
Place one capacitor per VCCO pin near the CY7B991 package. This should be physically closer than the 0.1uF cap.
C626 0.1uF
C621 0.1uF
C633 0.1uF
C627 0.1uF
C629 0.1uF
C634 0.1uF
Place one capacitor per VCCx pin near the CY7B991 package.
C614 10uF
Place between the two packages (CY7B991 & MPC947)
BUF4A_FDBK_MCLK35M
U6
CY2304-1
4 DSL1_SI_BUFMCLK
DSL1_BUF4_MR_MCLK 14
BUF4A_ROBOMCLK35M
BUF4A_BUF4B_MCLK
BUF4B_FDBK_MCLK35M
U5
BUF4B_DMR1_MCLK13
BUF4B_FG_DSL_MCLK 12
BUF4B_DMR2_MCLK13
Place one capacitor between pins 7 & 4 on each CY2304
C607 0.1uF
C596 0.1uF
R61 1.15k
R560 1.15k
U502
MPC947
4 MR_BUF_SCLK
R559 200
R60 200
BUF_DSL1_SCLK 4
BUF_DSL2_SCLK 5
BUF_DSL3_SCLK 6
BUF_DSL4_SCLK 7
BUF_DSL5_SCLK 8
BUF_DSL6_SCLK 9
BUF_DSL7_SCLK 10
BUF_DSL8_SCLK 11
BUF_FPGASCLK 13
BUF_DMR2_SCLK13
Place one capacitor per VCC pin near the MPC947 package
C27 0.1uF
C28 0.1uF
C21 0.1uF
C22 0.1uF
C25 0.1uF
C24 0.1uF
C23 0.1uF
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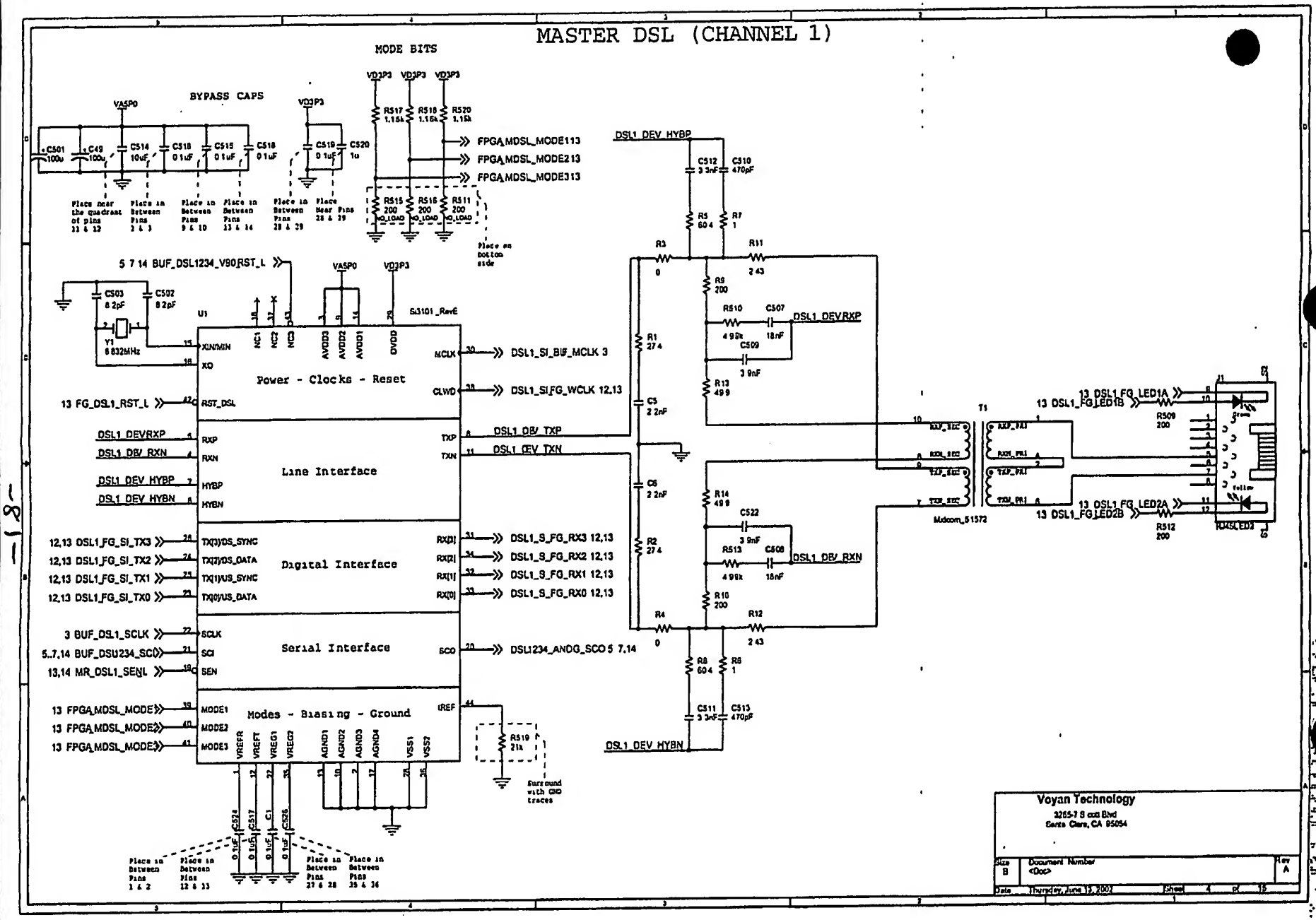
MASTER DSL (CHANNEL 1)
MODE BITS
BYPASS CAPS
VASP0
VD3P3
FPGA_MDSL_MODE1 13
FPGA_MDSL_MODE2 13
FPGA_MDSL_MODE3 13
DSL1_DEV_HYBP
DSL1_DEV_HYBN
5 7 14 BUF_DSL1234_V90_RST_L
U1
Power - Clocks - Reset
Lane Interface
Digital Interface
Serial Interface
Modes - Biasing - Ground
13 FG_DSL1_RST_L
DSL1_DEVRXP
DSL1_DEV_RXN
DSL1_DEV_TXP
DSL1_DEV_TXN
12,13 DSL1_FG_SI_TX3
12,13 DSL1_FG_SI_TX2
12,13 DSL1_FG_SI_TX1
12,13 DSL1_FG_SI_TX0
3 BUF_DSL1_SCLK
5..7,14 BUF_DSL1234_SCO
13,14 MR_DSL1_SENL
DSL1234_ANDG_SCO 5 7,14
Surround with GND traces
T1
Midcom_51572
13 DSL1_FG_LED1A
13 DSL1_FG_LED1B
13 DSL1_FG_LED2A
13 DSL1_FG_LED2B
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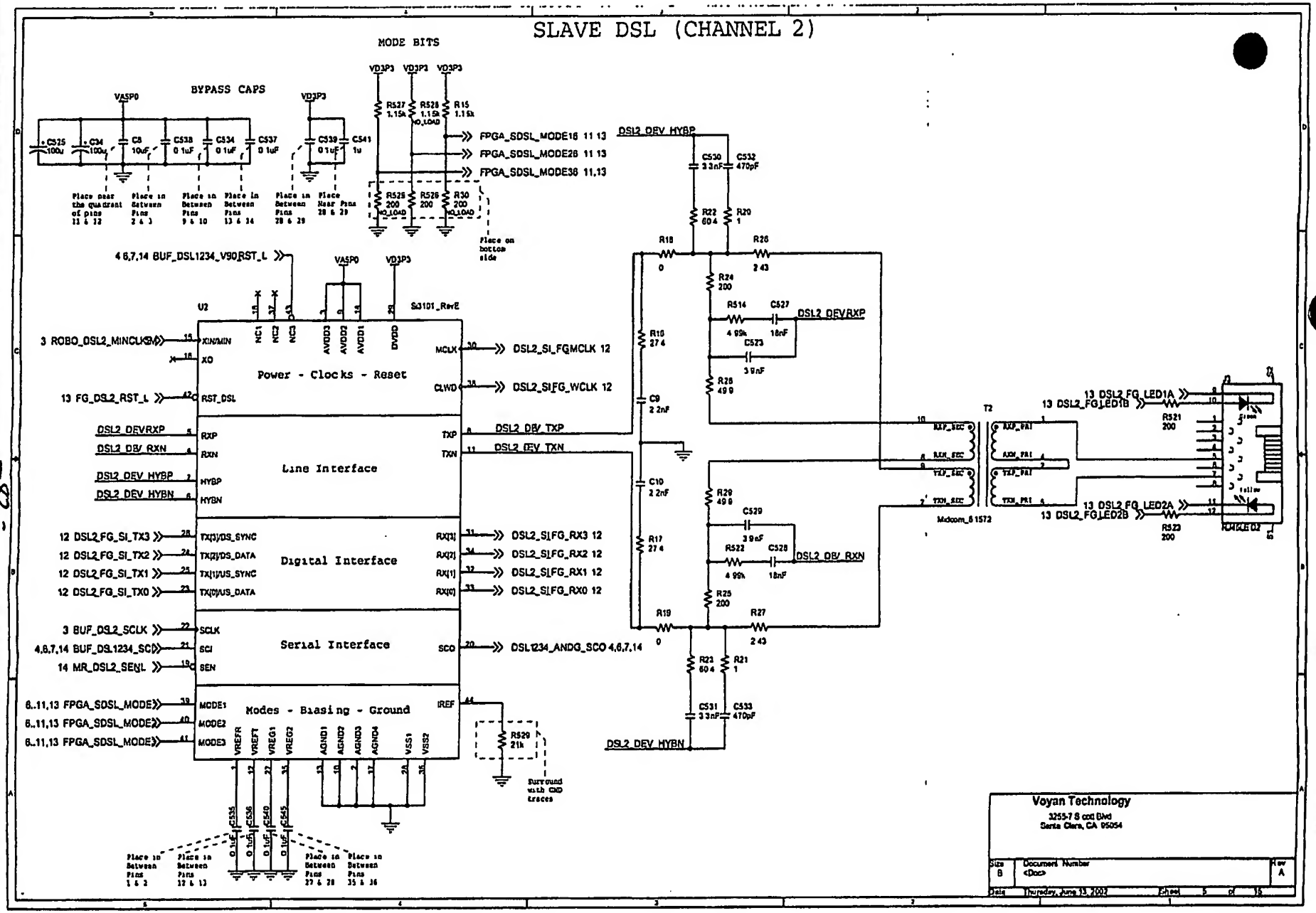
SLAVE DSL (CHANNEL 2)
MODE BITS
BYPASS CAPS
VA5P0
VD3P3
FPGA_SDSL_MODE1B 11 13
FPGA_SDSL_MODE2B 11 13
FPGA_SDSL_MODE3B 11,13
DSL2_DEV_HYBP
DSL2_DEV_HYBN
4 6,7,14 BUF_DSL1234_V90RST_L
U2
S3101_RevE
3 ROBO_DSL2_MINCLK
XIN/MIN
XO
RST_DSL
13 FG_DSL2_RST_L
Power - Clocks - Reset
MCLK
CLWD
DSL2_SI_FGMCLK 12
DSL2_SI_FG_WCLK 12
DSL2_DEVRXP
DSL2_DEV_RXN
DSL2_DEV_HYBP
DSL2_DEV_HYBN
RXP
RXN
HYBP
HYBN
Line Interface
TXP
TXN
DSL2_DEV_TXP
DSL2_DEV_TXN
12 DSL2_FG_SI_TX3
12 DSL2_FG_SI_TX2
12 DSL2_FG_SI_TX1
12 DSL2_FG_SI_TX0
TX[3]/DS_SYNC
TX[2]/DS_DATA
TX[1]/US_SYNC
TX[0]/US_DATA
Digital Interface
RX[3]
RX[2]
RX[1]
RX[0]
DSL2_SI_FG_RX3 12
DSL2_SI_FG_RX2 12
DSL2_SI_FG_RX1 12
DSL2_SI_FG_RX0 12
3 BUF_DSL2_SCLK
4,6,7,14 BUF_DSL1234_SCI
14 MR_DSL2_SENL
SCLK
SCI
SEN
Serial Interface
SCO
DSL1234_ANDG_SCO 4,6,7,14
6..11,13 FPGA_SDSL_MODE1
6..11,13 FPGA_SDSL_MODE2
6..11,13 FPGA_SDSL_MODE3
MODE1
MODE2
MODE3
Modes - Biasing - Ground
IREF
VREFR
VREFT
VREG1
VREG2
AGND1
AGND2
AGND3
AGND4
VSS1
VSS2
Surround with GND traces
T2
Midcom_61572
13 DSL2_FG_LED1A
13 DSL2_FG_LED1B
13 DSL2_FG_LED2A
13 DSL2_FG_LED2B
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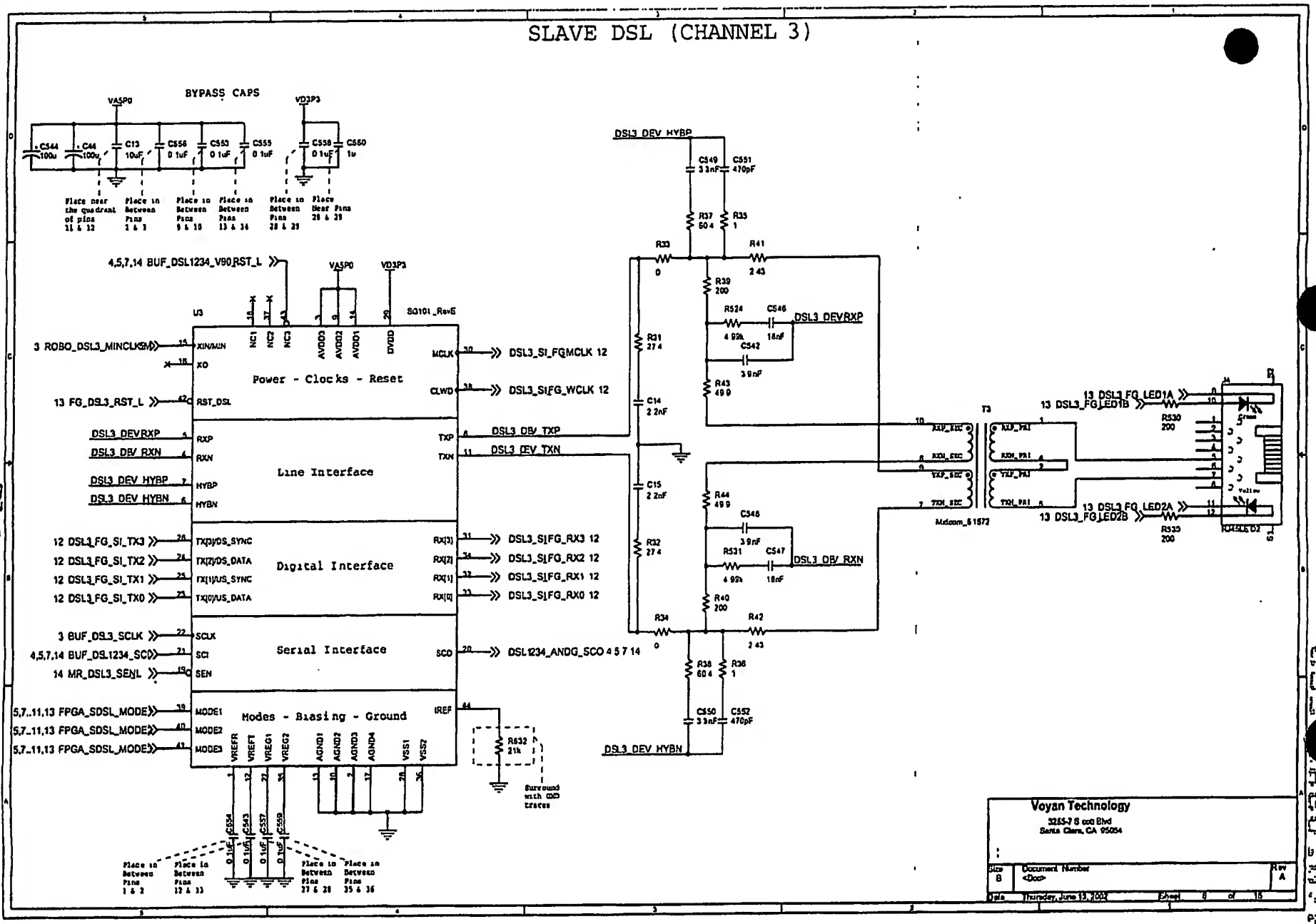

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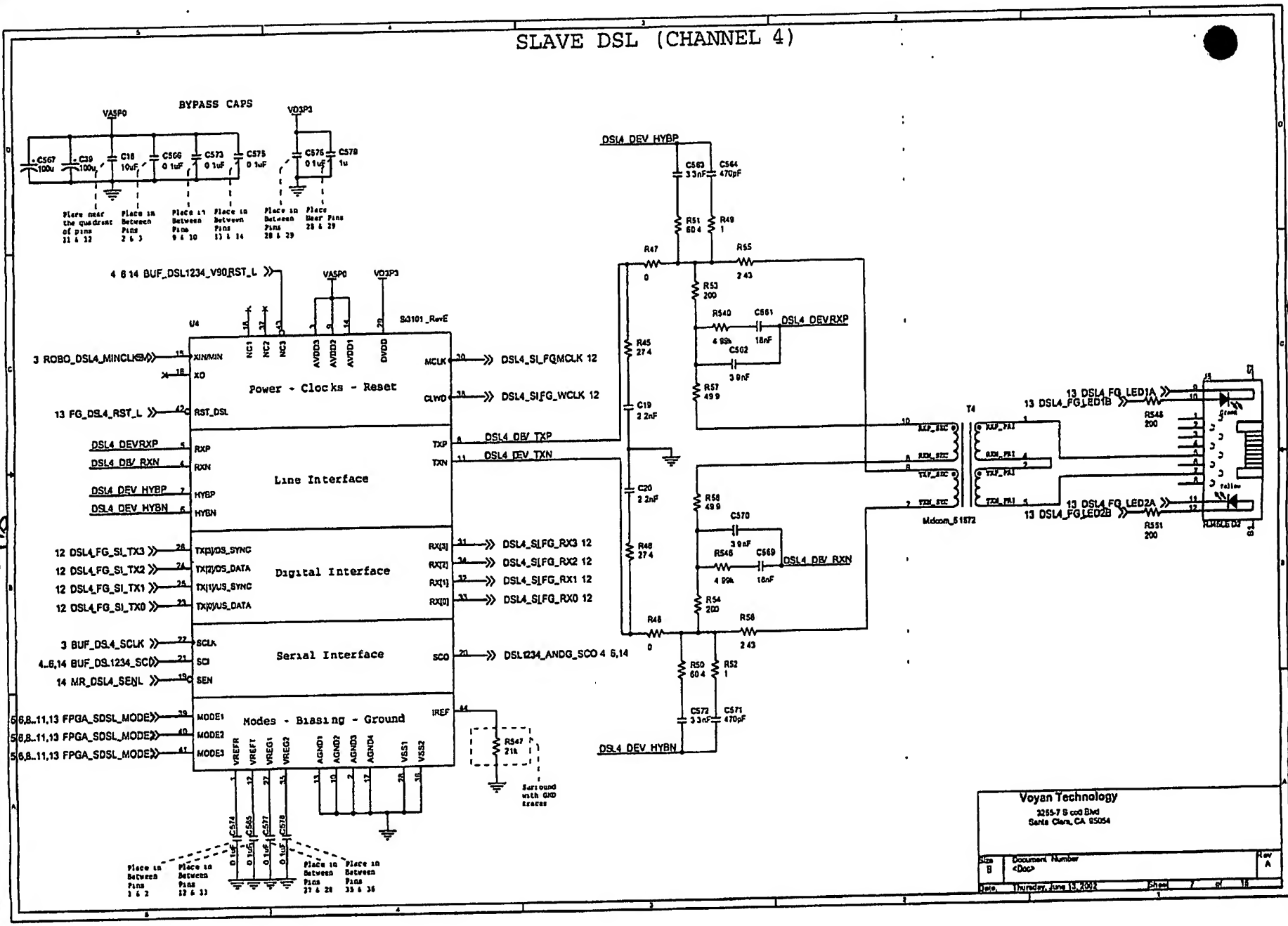
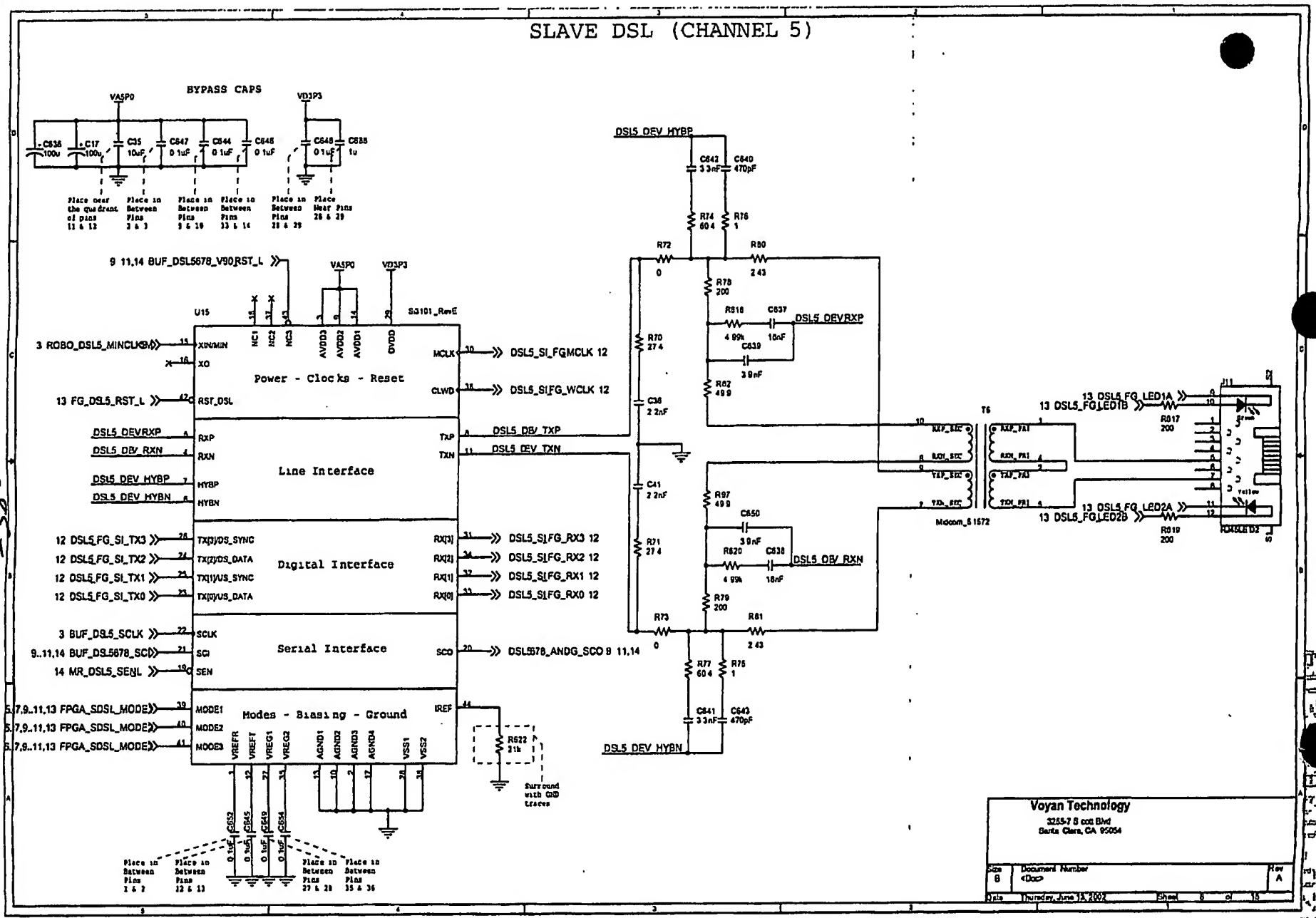


SLAVE DSL (CHANNEL 5)



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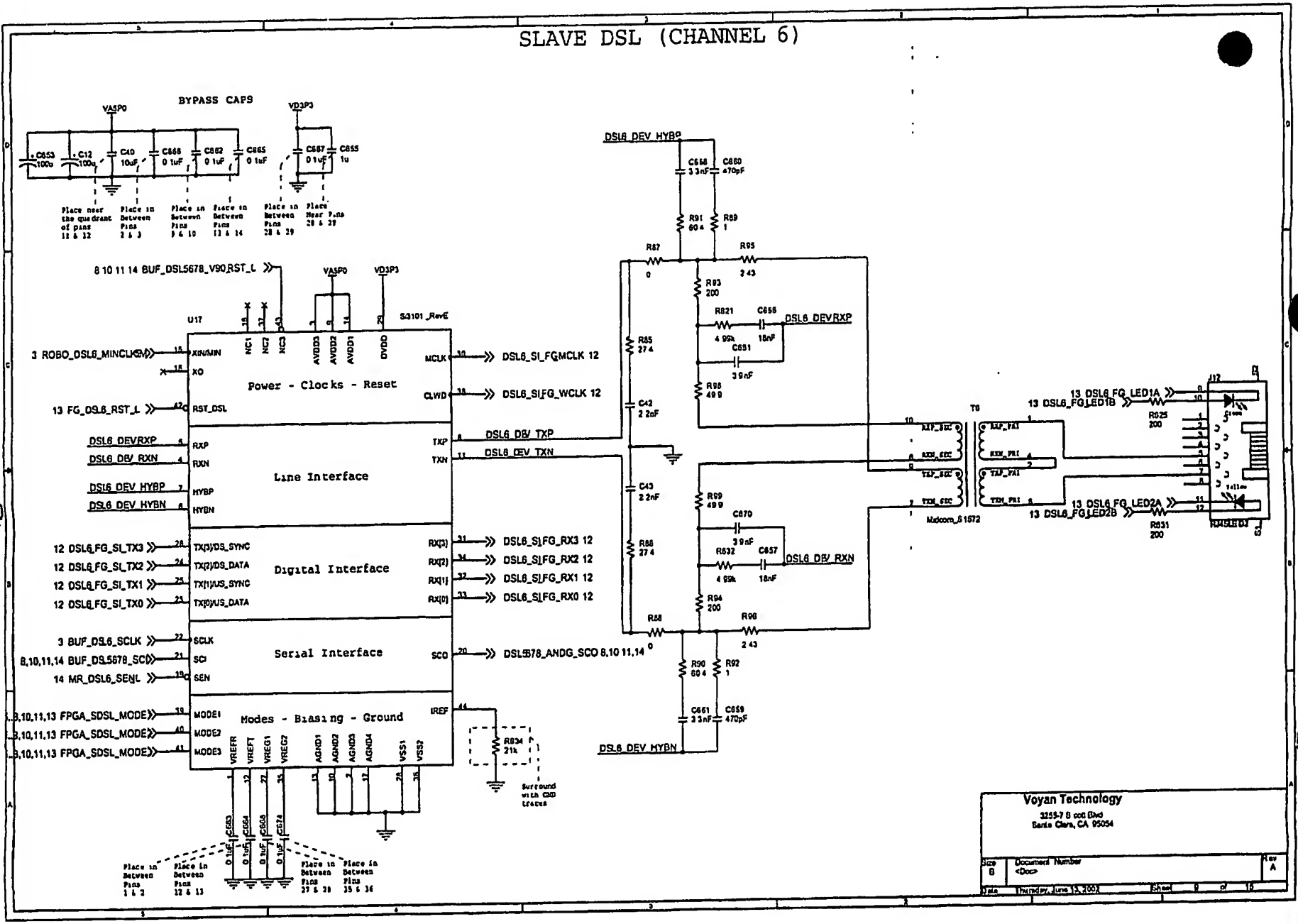

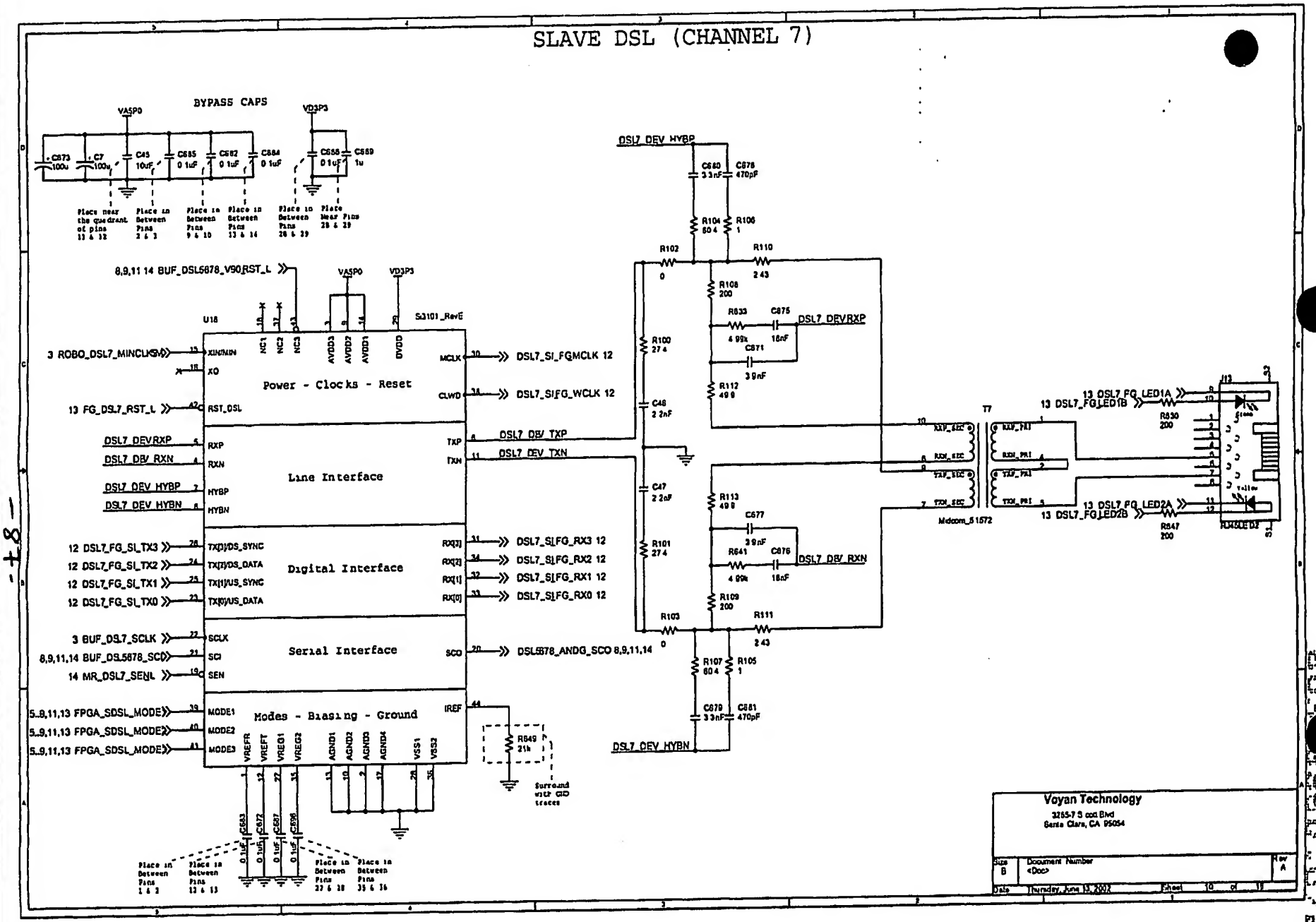
SLAVE DSL (CHANNEL 7)
BYPASS CAPS
VA5P0
VD3P3
C673 100u
C7 100n
C45 10uF
C685 0.1uF
C682 0.1uF
C684 0.1uF
C658 0.1uF
C659 1u
Place near the quadrant of pins 11 & 12
Place in Between Pins 2 & 3
Place in Between Pins 9 & 10
Place in Between Pins 13 & 14
Place in Between Pins 28 & 29
Place Near Pins 28 & 29
8,9,11 14 BUF_DSL5678_V90RST_L
U18
SI3101_RevE
NC1
NC2
NC3
AVDD3
AVDD2
AVDD1
DVDD
3 ROBO_DSL7_MINCLK
XIN/MIN
XO
13 FG_DSL7_RST_L
RST_DSL
Power - Clocks - Reset
MCLK
CLWD
DSL7_SI_FGMCLK 12
DSL7_SI_FGWCLK 12
DSL7_DEVRXP
DSL7_DEV_RXN
DSL7_DEV_HYBP
DSL7_DEV_HYBN
RXP
RXN
HYBP
HYBN
Line Interface
TXP
TXN
DSL7_DEV_TXP
DSL7_DEV_TXN
12 DSL7_FG_SI_TX3
12 DSL7_FG_SI_TX2
12 DSL7_FG_SI_TX1
12 DSL7_FG_SI_TX0
TX[3]/DS_SYNC
TX[2]/DS_DATA
TX[1]/US_SYNC
TX[0]/US_DATA
Digital Interface
RX[3]
RX[2]
RX[1]
RX[0]
DSL7_SI_FG_RX3 12
DSL7_SI_FG_RX2 12
DSL7_SI_FG_RX1 12
DSL7_SI_FG_RX0 12
3 BUF_DSL7_SCLK
8,9,11,14 BUF_DSL5678_SCO
14 MR_DSL7_SENL
SCLK
SCI
SEN
Serial Interface
SCO
DSL5678_ANDG_SCO 8,9,11,14
5..9,11,13 FPGA_SDSL_MODE0
5..9,11,13 FPGA_SDSL_MODE1
5..9,11,13 FPGA_SDSL_MODE2
MODE1
MODE2
MODE3
Modes - Biasing - Ground
IREF
R649 21k
Surround with GND traces
VREFR
VREFT
VREG1
VREG2
AGND1
AGND2
AGND3
AGND4
VSS1
VSS2
C683 0.1uF
C672 0.1uF
C687 0.1uF
C686 0.1uF
Place in Between Pins 1 & 2
Place in Between Pins 13 & 13
Place in Between Pins 27 & 28
Place in Between Pins 35 & 36
DSL7_DEV_HYBP
C680 3.3nF
C678 470pF
R104 604
R106 1
R102 0
R110 243
R108 200
R633 4.99k
C675 18nF
DSL7_DEVRXP
C671 3.9nF
R112 499
R100 274
C48 2.2nF
C47 2.2nF
R113 499
C677 3.9nF
R641 4.99k
C676 18nF
DSL7_DEV_RXN
R101 274
R109 200
R103 0
R111 243
R107 604
R105 1
C679 3.3nF
C681 470pF
DSL7_DEV_HYBN
T7
Midcom_51572
13 DSL7_FG_LED1A
13 DSL7_FG_LED1B
R550 200
13 DSL7_FG_LED2A
13 DSL7_FG_LED2B
R547 200
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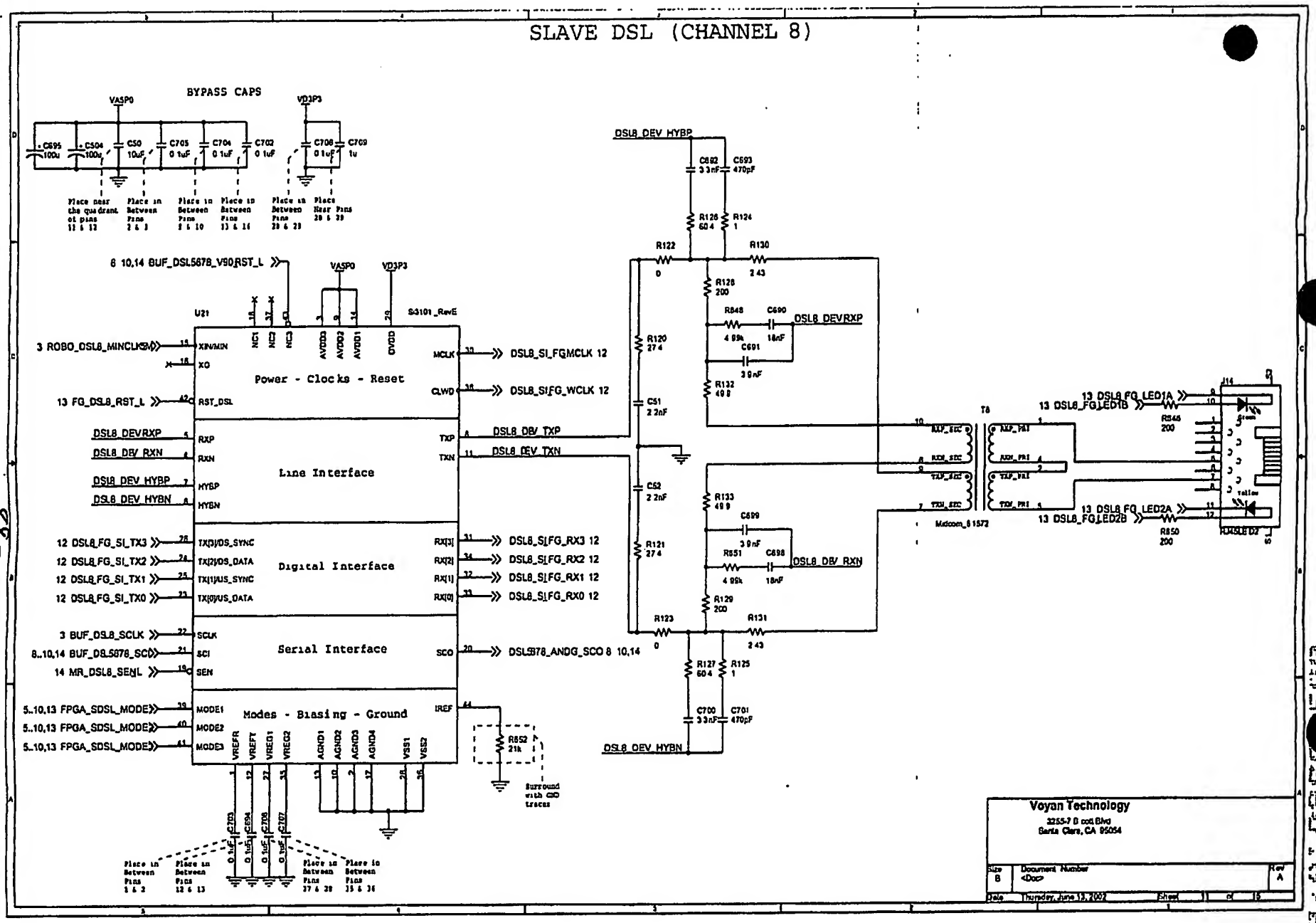
SLAVE DSL (CHANNEL 8)
BYPASS CAPS
VASP0
VD3P3
C695 100u
C504 100u
C50 10uF
C705 0.1uF
C704 0.1uF
C702 0.1uF
C706 0.1uF
C703 1u
Place near the quadrant of pins 11 & 12
Place in Between Pins 2 & 3
Place in Between Pins 8 & 10
Place in Between Pins 13 & 14
Place in Between Pins 28 & 29
Place Near Pins 38 & 39
8 10,14 BUF_DSL5878_V90RST_L
U21
S3101_RevE
3 ROBO_DSL8_MINCLKSM
13 FG_DSL8_RST_L
Power - Clocks - Reset
XIN/MIN
XO
RST_DSL
MCLK
CLWD
DSL8_SI_FG_MCLK 12
DSL8_SI_FG_WCLK 12
DSL8_DEV_RXP
DSL8_DEV_RXN
DSL8_DEV_HYBP
DSL8_DEV_HYBN
Line Interface
RXP
RXN
HYBP
HYBN
TXP
TXN
DSL8_DEV_TXP
DSL8_DEV_TXN
12 DSL8_FG_SI_TX3
12 DSL8_FG_SI_TX2
12 DSL8_FG_SI_TX1
12 DSL8_FG_SI_TX0
Digital Interface
TX[3]/DS_SYNC
TX[2]/DS_DATA
TX[1]/US_SYNC
TX[0]/US_DATA
RX[3]
RX[2]
RX[1]
RX[0]
DSL8_SI_FG_RX3 12
DSL8_SI_FG_RX2 12
DSL8_SI_FG_RX1 12
DSL8_SI_FG_RX0 12
3 BUF_DSL8_SCLK
8..10,14 BUF_DSL5878_SCI
14 MR_DSL8_SENL
Serial Interface
SCLK
SCI
SEN
SCO
DSL5978_ANDG_SCO 8 10,14
5..10,13 FPGA_SDSL_MODE1
5..10,13 FPGA_SDSL_MODE2
5..10,13 FPGA_SDSL_MODE3
Modes - Biasing - Ground
MODE1
MODE2
MODE3
VREFR
VREFT
VREG1
VREG2
AGND1
AGND2
AGND3
AGND4
VSS1
VSS2
IREF
R852 21k
Surround with GND traces
C703 0.1uF
C694 0.1uF
C708 0.1uF
C707 0.1uF
Place in Between Pins 1 & 2
Place in Between Pins 12 & 13
Place in Between Pins 27 & 28
Place in Between Pins 35 & 36
DSL8_DEV_HYBP
C692 3.3nF
C693 470pF
R126 604
R124 1
R122 0
R130 243
R128 200
R120 274
C51 2.2nF
R848 4.99k
C690 18nF
C691 3.9nF
DSL8_DEVRXP
R132 499
C52 2.2nF
R121 274
R133 499
C699 3.9nF
R851 4.99k
C698 18nF
DSL8_DEV_RXN
R129 200
R123 0
R131 243
R127 604
R125 1
C700 3.3nF
C701 470pF
DSL8_DEV_HYBN
T8
Midcom_81572
13 DSL8_FG_LED1A
13 DSL8_FG_LED1B
R846 200
13 DSL8_FG_LED2A
13 DSL8_FG_LED2B
R850 200
RJ45LED2
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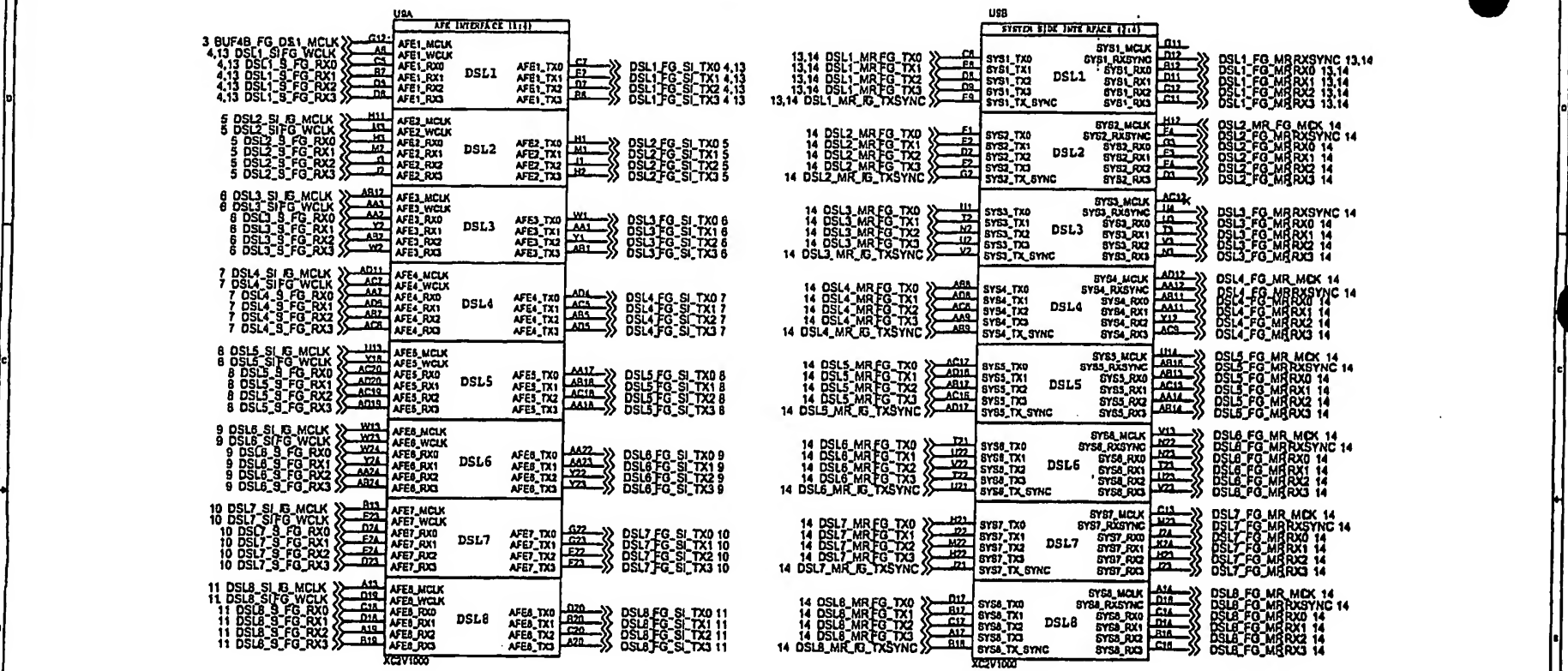

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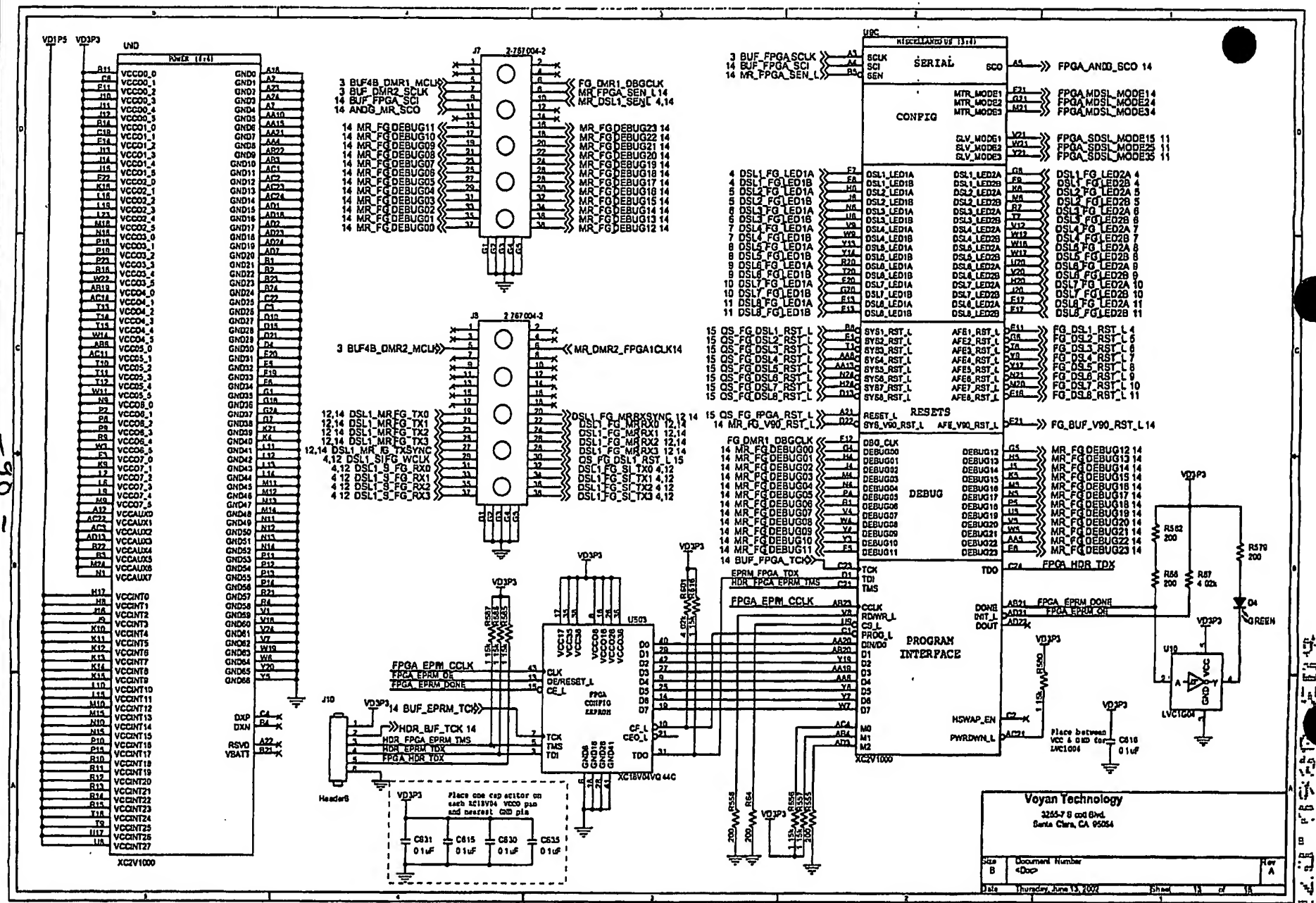
U9D
POWER (1 of 4)
XC2V1000
U9C
MISCELLANEOUS (3 of 4)
SERIAL
CONFIG
RESETS
DEBUG
PROGRAM INTERFACE
J7
J8
J9
J10
U503
XC18V04VQ44C
Header8
LVC1G04
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Santa Clara, CA 95054
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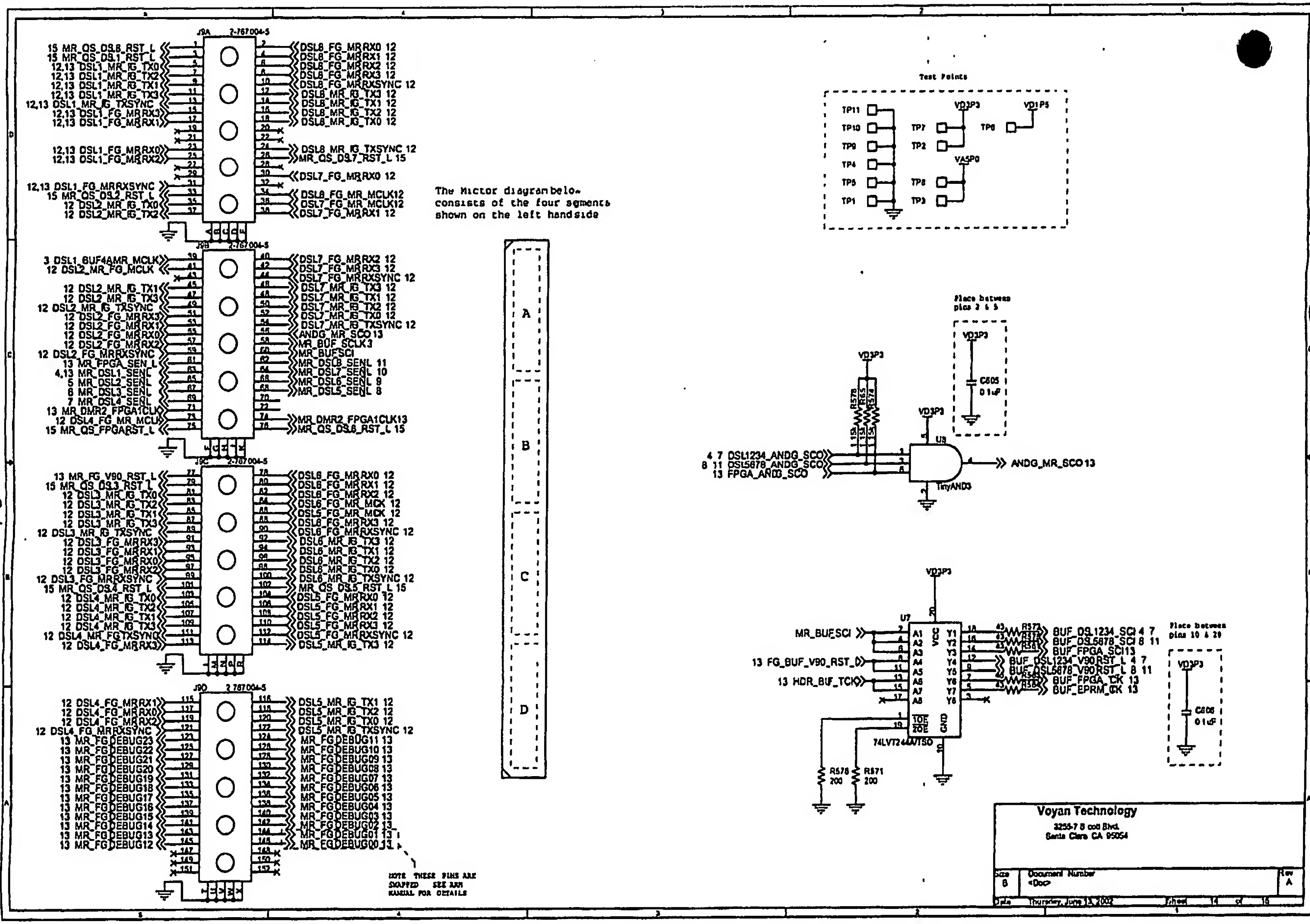

Test Points
TP11
TP10
TP9
TP4
TP5
TP1
TP7
TP2
TP6
TP8
TP3
VD3P3
VD1P5
VA5P0
The Mictor diagram below consists of the four segments shown on the left handside
A
B
C
D
J9A 2-767004-5
J9B 2-767004-5
J9C 2-767004-5
J9D 2-767004-5
Place between pins 2 & 5
C605 0.1uF
U8
TinyAND3
4 7 DSL1234_ANDG_SCO
8 11 DSL5678_ANDG_SCO
13 FPGA_AND3_SCO
ANDG_MR_SCO 13
U7
74LVT244AVTSO
MR_BUFSCI
13 FG_BUF_V90_RST_D
13 HDR_BUF_TCK
BUF_DS1234_SCI 4 7
BUF_DS5678_SCI 8 11
BUF_FPGA_SCI 13
BUF_DSL1234_V90RST_L 4 7
BUF_DSL5678_V90RST_L 8 11
BUF_FPGA_CK 13
BUF_EPRM_CK 13
R578 200
R571 200
Place between pins 10 & 20
C606 0.1uF
NOTE THESE PINS ARE SWAPPED SEE XXX MANUAL FOR DETAILS
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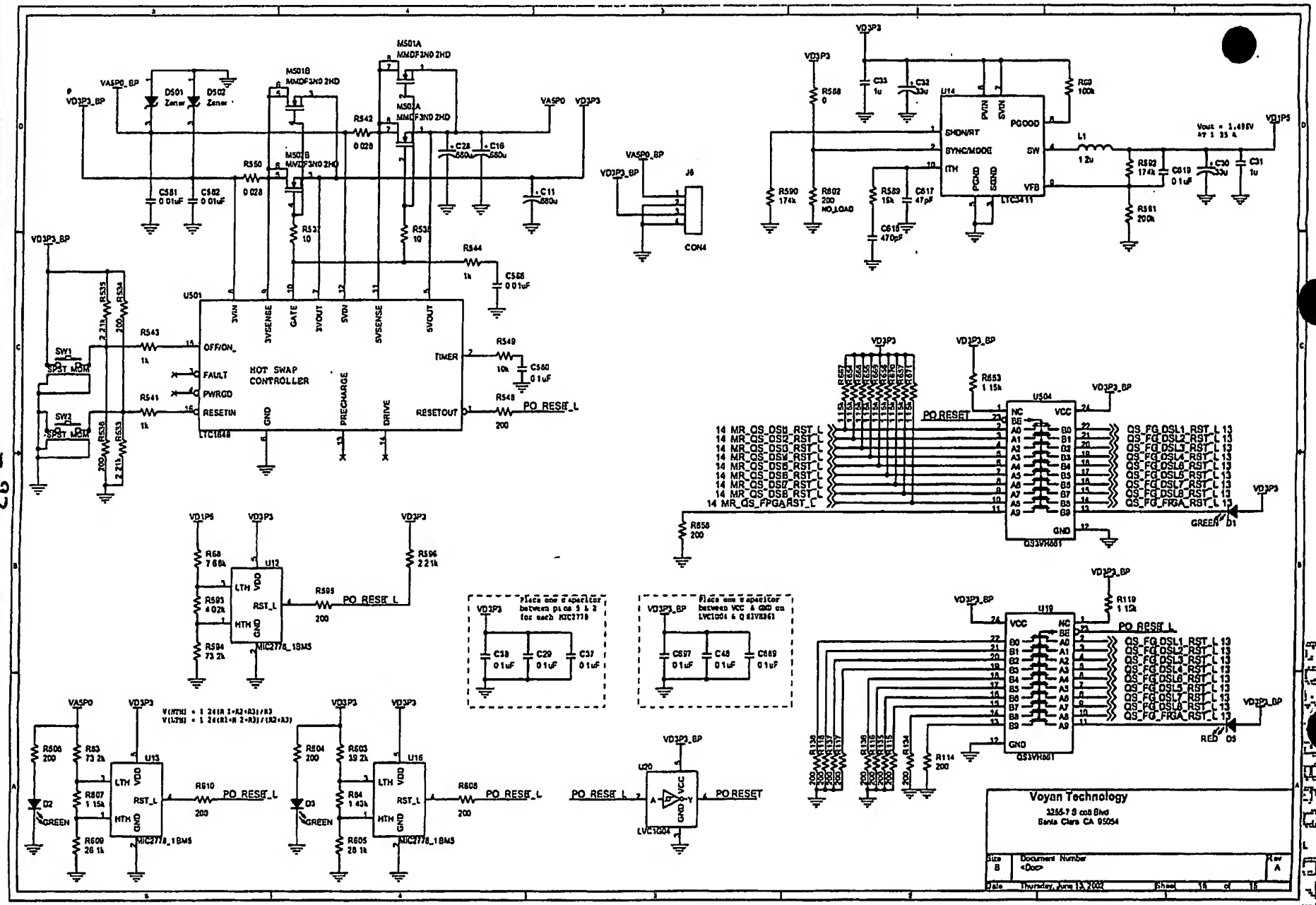
HOT SWAP CONTROLLER
LTC1648
LTC3411
Q3IVH561
MIC2778_1BMS
LVC1G04
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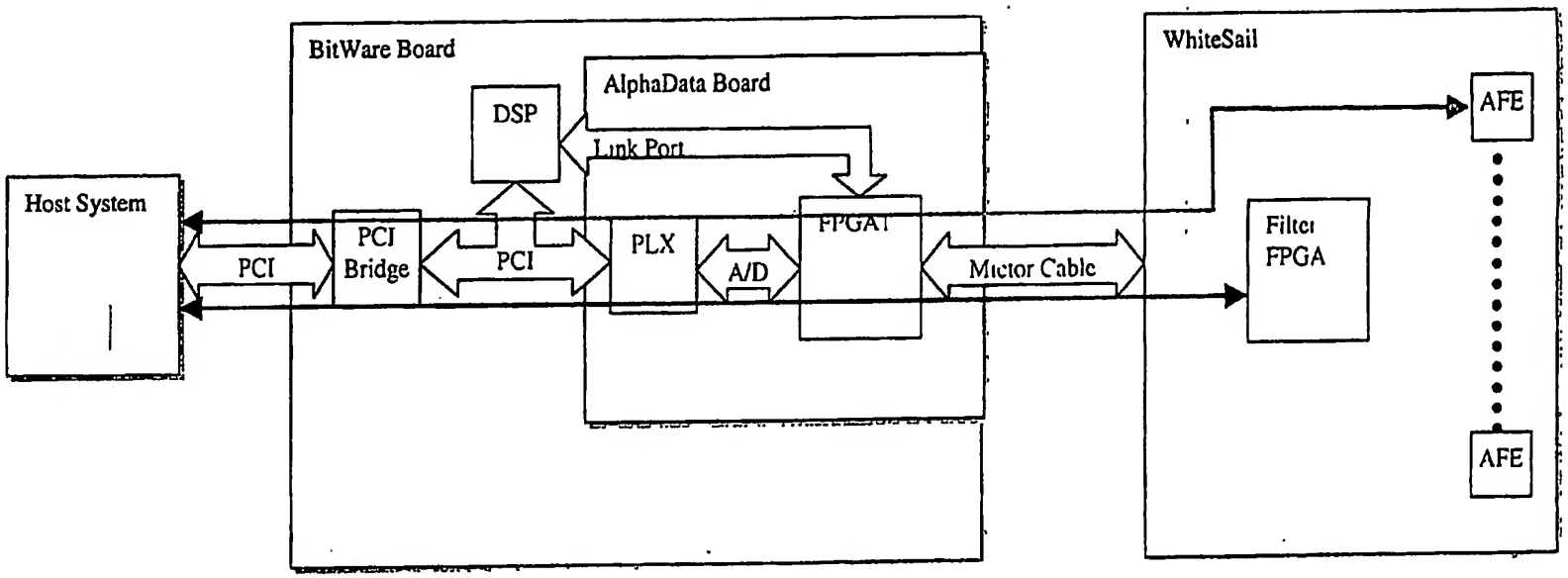
Test 1 – Register Access:

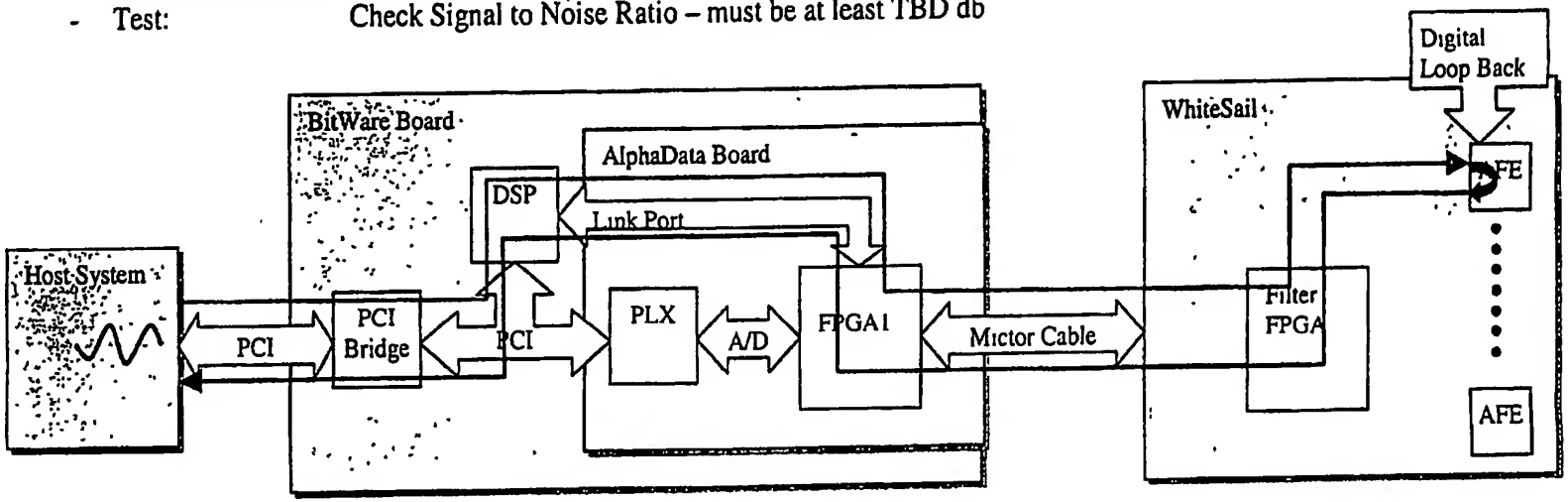


Differences to hardware:

- Clocking is provided by master SiLabs part, instead of external VCXO
- Register access to AFE chips is directly from FPGA1 to AFE chip through Mictor cable, instead of going through filter FPGA

Test 2 – SNR Test with Digital Loopback

- Settings: Digital Loop Back (LB2 = 1)
- Input: 69 kHz sinusoid, full scale
- Output processing: 1024 length FFT
- Test: Check Signal to Noise Ratio – must be at least TBD db

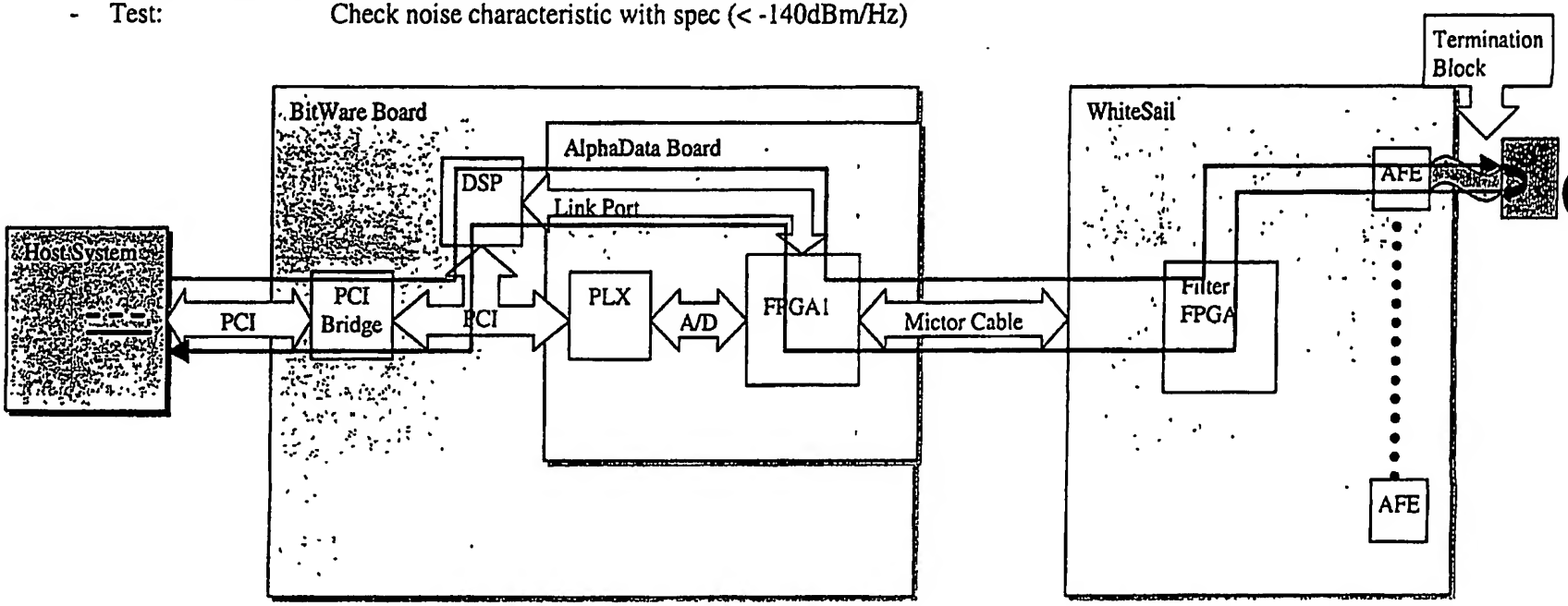


Differences to hardware:

- Clocking is provided by master SiLabs part, instead of external VCXO.
- Data interface from FPGA1 to Filter FPGA is different.

Test 3 – Noise Characteristic Test

- Settings: Nominal, RxGain = 26dB
- Input: DC (all 0's)
- Output processing: 1024 length FFT, with appropriate scaling (line-referenced)
- Test: Check noise characteristic with spec (< -140dBm/Hz)

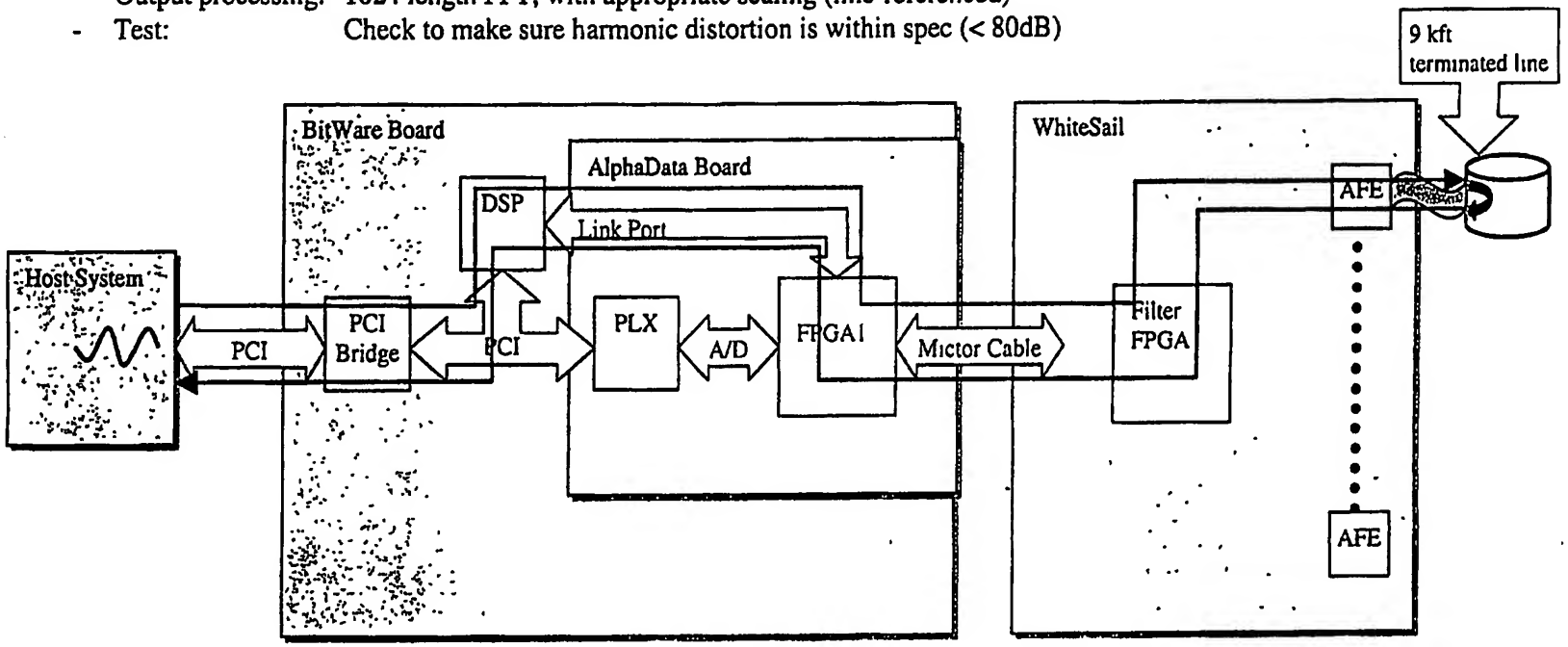


Differences to hardware:

- Clocking is provided by master SiLabs part, instead of external VCXO.
- Data interface from FPGA1 to Filter FPGA is different.

Test 4 – Harmonic Distortion Test

- Settings: Nominal, RxGain = 12dB
- Input: 69 kHz sinusoid, ¼ full scale
- Output processing: 1024 length FFT, with appropriate scaling (line-referenced)
- Test: Check to make sure harmonic distortion is within spec (< 80dB)

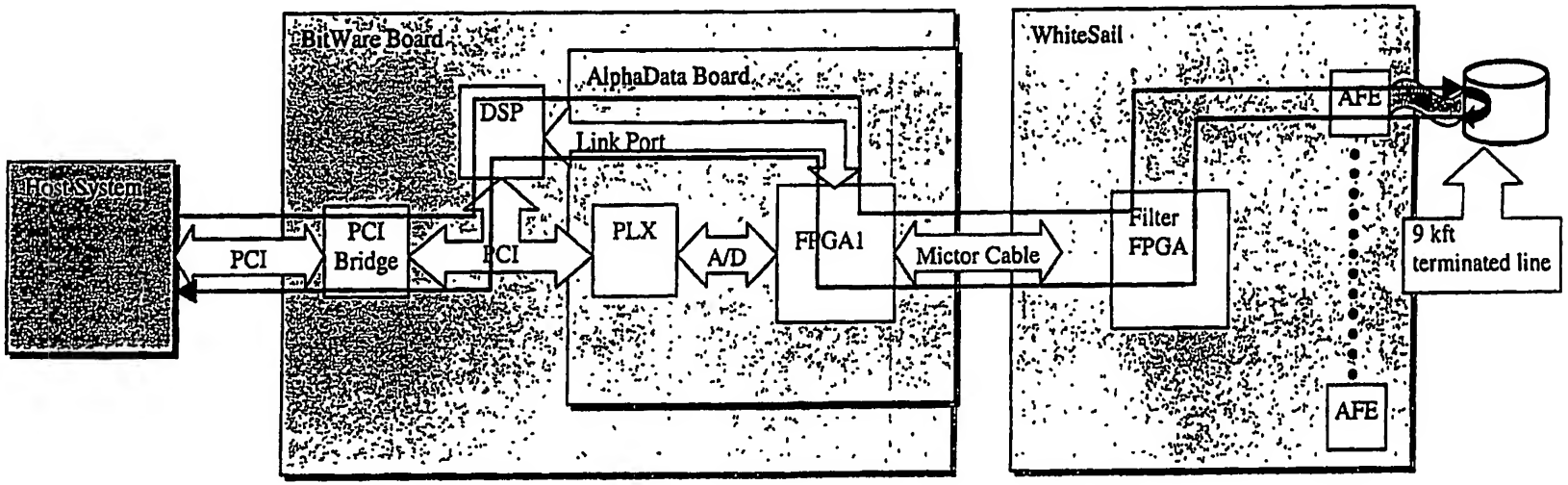


Differences to hardware:

- Clocking is provided by master SiLabs part, instead of external VCXO.
- Data interface from FPGA1 to Filter FPGA is different.

Test 5 – Final Echo Rejection Test

- Settings: Nominal
- Script: Run gsafixed script (GSA = Geodesic Search Algorithm)
- Input: Reverb signal specified by script
- Output processing: Several – FFT, Variance, etc. (all Matlab routines)
- Test: Check to make sure final echo rejection is within spec: –18 dB to –28 dB (linear slope in dB) from 10 kHz to 130 kHz, –28 dB from 125 kHz to 400 kHz, –28 dB to –18 dB (linear slope in dB) from 400 kHz to 550 kHz

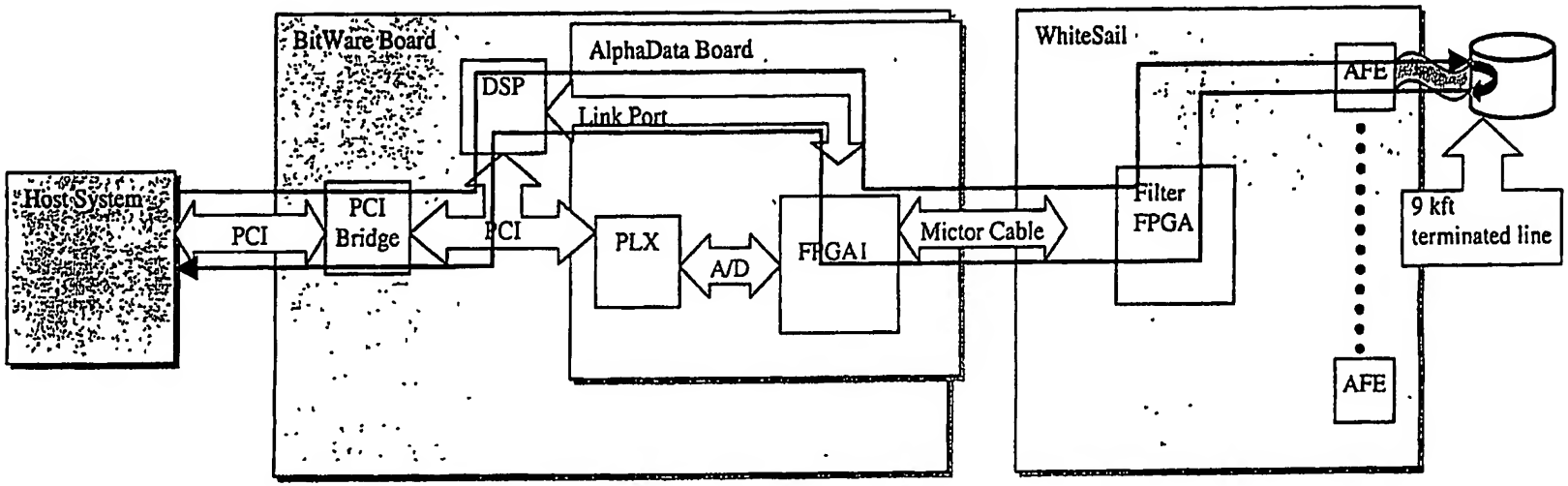


Differences to hardware:

- Clocking is provided by master SiLabs part, instead of external VCXO.
- Data interface from FPGA1 to Filter FPGA is different.

Test 6 – Internal VCXO Clock Jitter Test and Master Clock Adjustment

- Hardware: Single WhiteSail Board
- Script: Only the script that sets FPGA1 register value for VCXO.
- Input: Selected VCXO control register values from 0x000 to 0xFFF
- Equipment: Spectrum Analyzer
- Test: Check to make sure that the nonlinear effect of VCXO follows the Figure 13 on Silab Chip Spec and adjust the master clock frequency to the linear range.

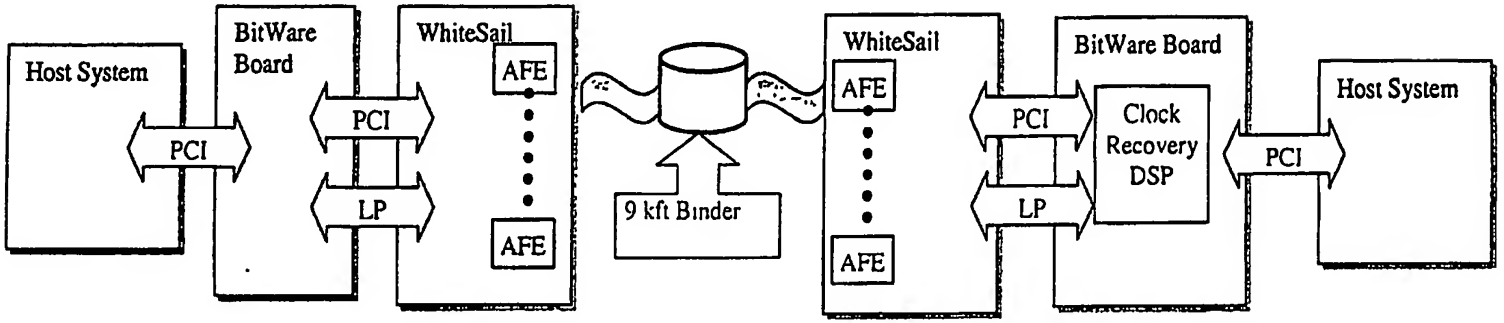


Differences to hardware:

- Clocking is provided by master SiLabs part, instead of external VCXO.
- Data interface for VCXO control loop is different.

Test 7 – VCXO Closed-loop Performance Test

- Settings: Two WhiteSail Boards (Master and Slave) connected through 9kft loop.
- Script: Run the clock recovery DSP and Matlab routine in Build 5 (Simplex)
- Input: Reverb signal specified by script for clock recovery
- Output processing: Several – Phase Noise, Clock Jittering, etc. (all Matlab routines)
- Test: Check to make sure the closed-loop clock jittering falls within the specification: 1e-3 of sample period.



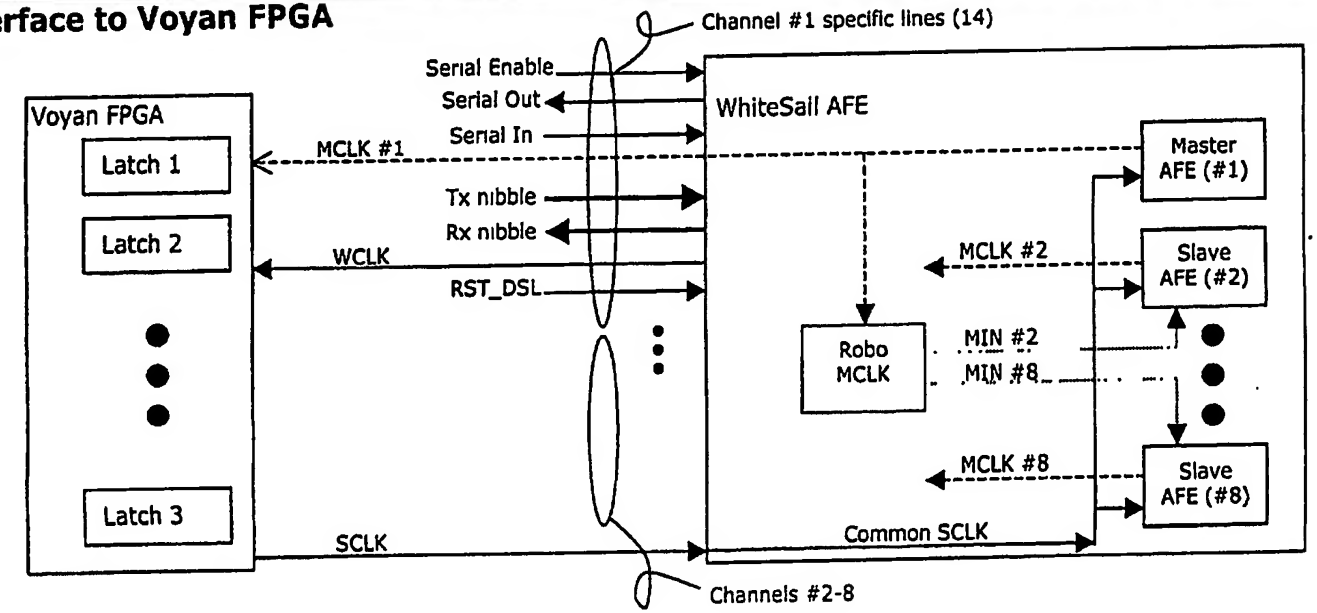
Differences to hardware:

- Clock recovery uses internal VCXO on SiLab Chip.
- No DAC, external VCXO, etc.

Differences to software:

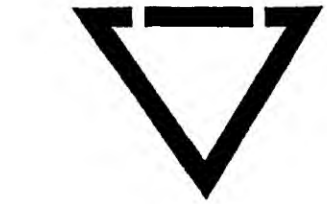
- DSP Mapping function. DSP clock recovery code needs to be updated to reflect the mapping relation for the internal VCXO control: 0x000-0xFFF corresponding to –100 to 100 ppm (with capacitor = 8.2pF).

1. Interface to Voyan FPGA



Notes:

- AFE device is a Silicon Labs Si3101. There are 8 of these devices on the board.
- Board form factor is Compact PCI 6U rear-board (80 mm x 220 mm).
- AFE channel 1 MCLK (master clock output) is used to source the MIN (master clock input) for all other channels. Channel 1 VCXO is internal, Channels 2-8 are external through Robo MCLK.
- SCLK is common to all AFE channels.
- MCLK #1-8 must interface to Xilinx clock input lines.
- Connector is Mictor 146 pin. Voyan to provide mapping of these signals (14*8+1) to pinout.



Demonstration Hardware

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2. Hardware Elements

2.1 System overview

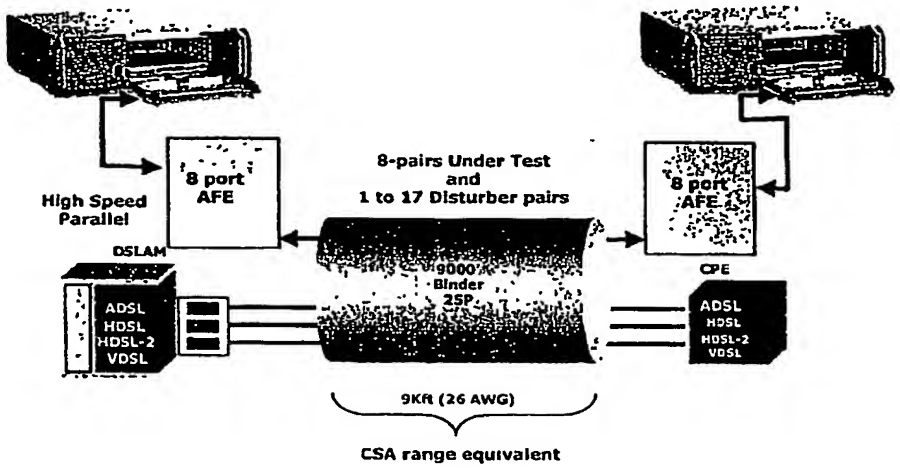

Fig. 1 System overview

The Demonstration system consists of two demonstration platform which communicate over eight copper pair of an actual 26AWG binder. Cable of lengths of 9000 feet of 26AWG can be connected. In order to prove system performance under a variety of real-world conditions, a number of disturbance services can be introduced into the same binder, in order.

This document will outline the hardware available in the lab to create these disturbance conditions.

2.2 Loop Plant

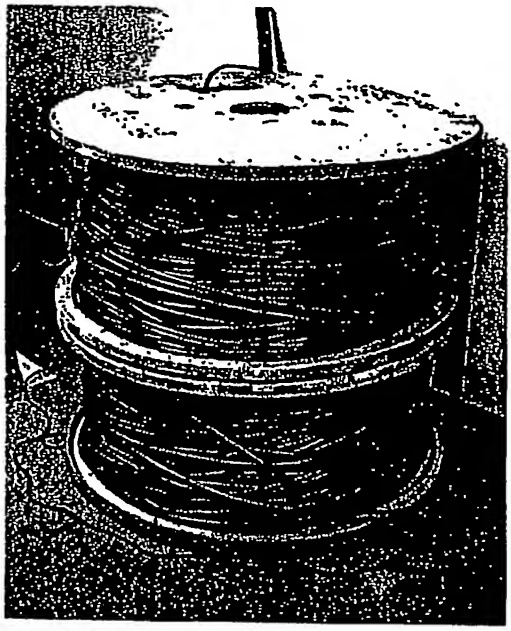

Fig. 2: 26AWG Cable

The following lengths of real cable are available in the lab:

- 26AWG loops (9kft in total).
  - 1kft x 2 loops.
  - 3kft.
  - 4kft.
- 24AWG.
  - 1kft x 2 loops.

The focus of the demonstration is on CSA range of 26AWG cable.

2.3 Patch Panels

There are two patch panels systems in the lab one for each type of cable. These allow for various lengths of smaller cable may be linked together to form longer cable reaches. Of these the 26AWG patch panel is the most utilized. Fig. 2 illustrates the 26AWG patch panel

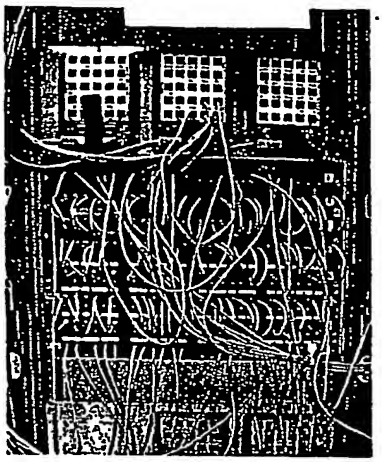

Fig. 2: 26AWG patch panel

Fig. 3 illustrates how the various loops of cable are wired to the patch panel. It is easy to see that by daisy chaining the twisted pair from each loop together, up to 9000kft of cable can be formed.

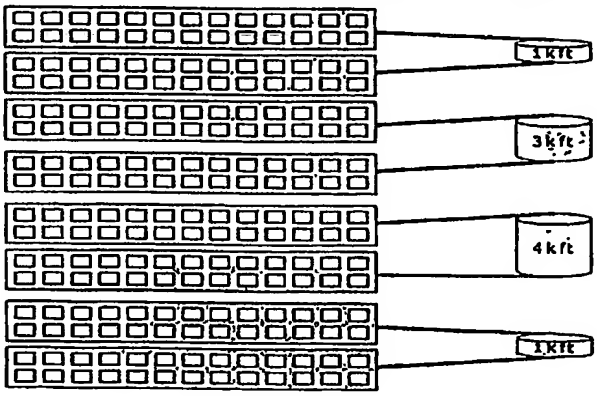

Fig. 3: 26AWG patch panel wiring

It is easy to see how a daisy chain arrangement on the patch panel allows for the concatenation of individual loops of cable up to a maximum length of 9000 feet. It also allows for the addition of bridge taps at intervals corresponding to the patch panel intervals.

A similar but much simpler patch panel exists for the 24AWG cable, basically allowing the connection of the two 1kft loops of cable.

2.4 Disturber sources

The disturber scenarios are realized by activating disturber services within the loop plant. A variety of equipment is used to each type of disturbance.

2.5 HDSL Disturbance

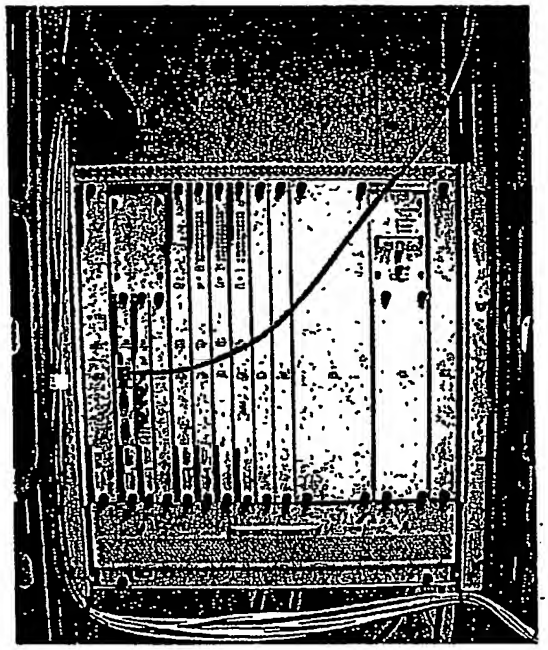

Fig. 4: Copper Mountain CopperEdge DSLAM

The is SDSL DSLAM is adjustable to different rates, thereby enabling emulation of different services such as HDSL and ISDN. Currently we use SDSL to mimic the power spectrum of HSDL.

- DSLAM: Copper Mountain: CopperEdge.
  - 24 SDSL ports (currently 5 used).
    - Currently use 5 system ports.
      - 1 to mimic ISDN.
      - 4 to generate a power spectrum compatible to HDSL.
  - 24 ADSL ports (currently not used).
  - 24 G.lite ports (currently not used).
- Modem: CopperRocket SDSL modem.
  - 5 units used as counterparts to 5 DSLAM ports.
  - A further 7 units are in-house but unused.

2.6 ADSL Disturbance

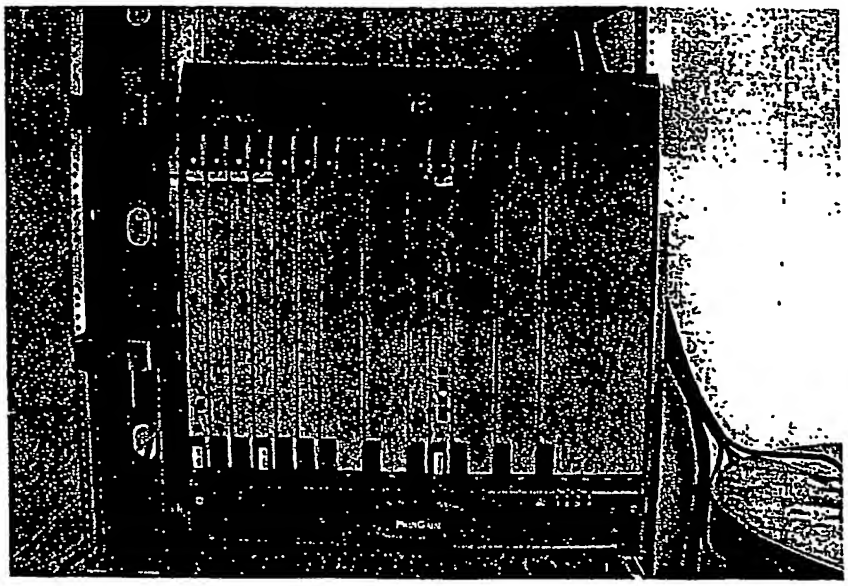

Fig. 5: AVIDIA 8000 DSLAM

- DSLAM: AVIDIA 8000 (Fig. 5).
  - 12 ADSL ports (currently 3 used).
  - 48 SDSL ports (proprietary SDSL – power spectrum not compatible to HDSL).
- Modem: Pairgain MEGABIT MODEM 600F.
  - 3 units.

ADSL service is run at 640 kbps downstream / 64 kbps upstream.

2.7 DDS Disturbance

- DDS terminal: Multitech MultiDSU64K.
  - 2 units run point to point.
  - Run in "PRBS test-mode' which mimics a real-world data transmission conditions.

2.8 HDSL2 Disturbance

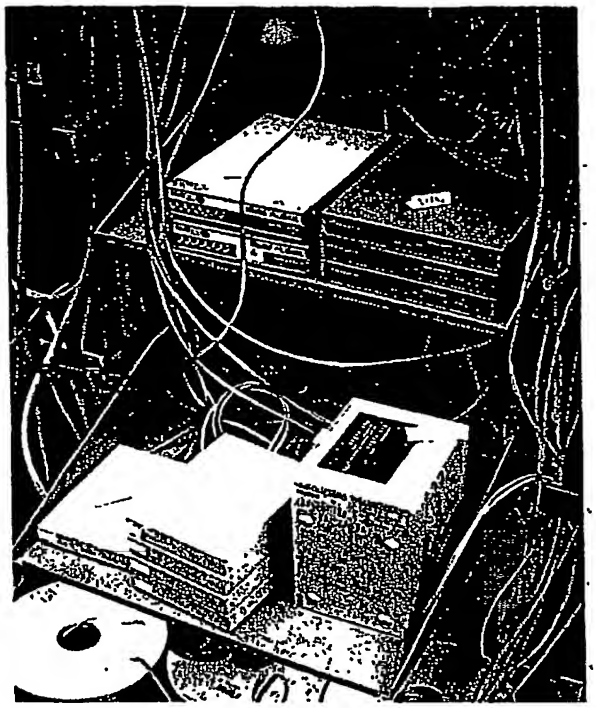

Fig. 6: CPE modems, including Pairgain HDSL2 remote enclosure (bottom right)

The HDSL2 disturbance is realized using a Pairgain system which consists of DSU and CSU

- DSU: Pairgain HiGain Solitare
  - 2 linecards – 1 port per card
- CSU: Pairgain HRE 204 (Fig. 6)
  - 2 ports

2.9 VDSL Disturbance

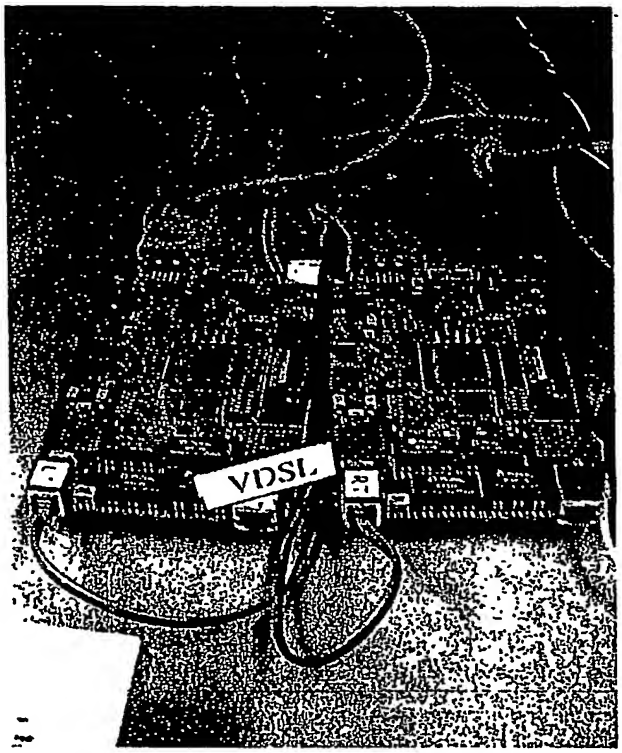

Fig. 7: Infineon IVES VDSL chipset evaluation boards

- Infineon IVES 22812 evaluation system (Fig. 7)
  - Contains Infineon's 2nd generation VDSL chipset.
  - Consists of two boards, one in Line Termination mode, one in Remote Terminal mode connected point to point to realize the VDSL connection.
  - connected over 1kft of cable (at the CPE end of the cable).

3.0 Demonstration

The focus of this demonstration is on raw throughput over various reaches in the presence of various disturber scenarios. As such the demonstration system doesn't not

Performance under four disturbance scenarios will be demonstrated. These disturbance scenarios are detailed in the following table.

Disturbance source	Zero	Light	Medium	Heavy
ADSL	0	1	2	3
HDSL	0	1	2	2
HDSL2	0	1	2	2
VDSL	0	1	1	1
DDS	0	0	1	1
ISDN	0	0	0	1
# External Disturbers	0	5	11	13

Fig. 8: Disturbance Scenarios

CLAIMS

What is claimed is that which has been described in the foregoing and equivalents thereof.

[redacted]

ABSTRACT

A method and system are disclosed using multi-lines to deliver ultra high speeds in a communications system.